HIGH GAIN NARROW BAND LNA DESIGN FOR Wi-MAX APPLICATIONS AT 3.5GHZ

A Thesis submitted in partial fulfillment of the Requirements for the degree of

Master of Technology

In

Electronics and Communication Engineering

Specialization: VLSI Design & Embedded System

By

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Dedicated to…

My Well Wishers

DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING

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CERTIFICATE

This is to certify that the work in the thesis entitled **High gain Narrow band LNA design for Wi-MAX applications at 3.5GHz** by **Naveen Motamarri** is a record of an original research work carried out by him during 2013 - 2014 under my supervision and guidance in partial fulfillment of the requirements for the award of the degree of Master of Technology in **VLSI Design & Embedded System** (Electronics and Communication Engineering), from National Institute of Technology, Rourkela. Neither this thesis nor any part of it, to the best of my knowledge, has been submitted for any degree or diploma elsewhere.

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Abstract

The wireless communication has been experiencing tremendous growth in technology. The demand has been increased for low cost RFIC designs. Many researches are going on front end design of RF transceiver. The design of receiver path has become a challenging aspect, because of increased interferences around the communication path. Transmitter path design is easy because interference levels are very less compared to signal level. As the operating frequency is higher in RFIC design, receiver path also experiencing the internal noises in the system. The performance of transceiver depends on each of the individual blocks such as low noise amplifiers.

In this thesis, Two RF CMOS narrow band LNAs (cascode, differential) are designed. They are designed for the IEEE 802.16 standard in the 3.5 GHz band for Wi-MAX applications. Low noise amplifier is used as the first block after the receiving antenna. This LNA is placed before the mixer in the receiver path for amplification. The LNA must have good gain and low NF to avoid further degradation of receiver path. This thesis focuses on design of a high gain LNAs with acceptable noise figure operating at 3.5GHz. Inductive Source degeneration method is used to match the circuit to source impedance in all the designs. All the circuits operate with 1.8v supply voltage. Here in this thesis, Enhanced cascode LNA exhibits a gain of 26.88dB and NF of 2.55dB and the Differential LNA exhibits a gain of 32.71dB and NF of 2.66dB. The circuits are designed using cadence 0.18µm RF CMOS technology.

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INTRODUCTION

1.1 Motivation

The traffic of audio and video based messages has grown in recent years. Which, led to the need for even gradually higher data-rates for the next generation wireless communication applications. The cellular telephony and wireless local area networks (WLANs) are the two prime directions and in recent years, realization of fully integrated system-on-a-chip (SoC) has become a major interest in receiver front end design architectures while retaining low cost. This is the main reason for the Complementary Metal-Oxide Semiconductor (CMOS) technology to be very popular in RF circuit designs.

The interest has grown towards technologies which can offer higher data rates in large global areas. Wi-Max can provide wide range, large bandwidth and lower cost of data rates. IEEE 802.16 standards is named as Wireless MAN by IEEE. It is eventually known as Wi-MAX. Wi-MAX Forum cited 2.3, 2.5 and 3.5GHz frequencies for standardization. A significant amount of research work has been done at 2.5GHz, because of its widespread global usage. Though, not much amount of work is stated in research or industrial for 3.5GHz, though it is much needed spectrum in many other uses, especially for the reason of the authorizing requirements.

Wi-MAX can provide 30 - 40MBPS data rate, now a days providing upto 1GBPS. The standard "Wi-MAX" was created by Wi-MAX Forum, and was particularly designed to serve the fundamental network layers of wireless personal area network (WPAN) which concentrates on low-cost, low-speed communication between devices. The focus is on very low cost communication to nearby devices without less power consumption and small underlying infrastructure. The LNA also used in W-CDMA applications at 3.5GHz.

- It is providing broadband connectivity across cities and countries for portable mobile through a variety of devices.
- It can provide a wireless communication to cable and digital subscriber line (DSL) aimed at "last mile" broadband access.
- It also can provide data, telecommunications (VoIP) and IPTV services at low cost.

- Provides a source for Internet connectivity in a business continuity plan.

Wi-MAX can provide mobile Internet access at home or across whole cities to countries. In many cases this has been resulting in competition in market which typically had access with the help of an existing incumbent DSL operator.

Moreover, given the comparatively low costs associated with the use of WiMAX networks (in contrast with 3G, HSDPA, and HFC or FTTx). Wi-Max is now economically capable to provide last mile Internet access at remote locations.

1.2 LITERATURE REVIEW

The cascode LNA is the widely used architecture among the LNA designs. This Cascode architecture fulfills all the requirements for the low noise amplifier design. This cascode LNA still has a problems like trade-off between Gain- noise figure, input matching and noise figure, load tuning and output matching. And the cascade CG stage will generate some amount noise even though it is used to provide better isolation. The parasitic capacitances around the CS-CG stages degrade the noise performance. In the paper[13] Wei Li, Chao Shiun and Chorng proposed Complementary Switched Capacitor multi band LNA design at 2.4GHz/3.5GHz/5GHz in 0.18um CMOS, but this design has problems like high noise figure and low forward gain at one of the three frequencies. There is no proper input matching at all the frequencies either. A few designs were done at 3.5GHz, A narrow band 3-5GHz LNA design made by Siti Maisurah, Wong Sew Kin, Fabian Kung and See Jin Hu. The design doesn't have proper input and output matching. A similar Ultra wide band design is done from 2.9 - 3.5GHz by Chong-Ru Wu and Liang-Hung Lu , but with bad input/output matching.

A very simple approach to attain a low noise figure and proper load matching and to overcome these difficulties can be done through a series resonate inductor described in [8]. This is introduced between the two stages (CS-CG) to remove all the parasitic capacitance effects. And a buffer stage is placed after output stage to get off the tradeoff between tuning the load and matching the output. This simple steps gives the better gain, proper output matching and improved noise figures.

1.3 NARROW-BAND RECEIVER

1.3.1 Introduction to Narrow-Band Receiver Systems

The design of integrated radio frequency (RF) receiver circuit needs a combination of expertise in the circuit design areas, system design architecture, and technology process. One of the most widely used receiver types is the narrow-band receiver as many of wireless networking architectures are mostly based on it. So, the need for wireless transceiver circuits operating in the GHz band range has become extensive.

Research on the corresponding system architectures as well as on the integrated circuit designs those implement precise transceiver functions. Though, the performance of such transceiver circuits mainly depends on that of each of the single individual blocks. Also, the quality and range of the communication links is mainly determined by the electrical performance of transmitter and receiver. These two qualities, as well as the cost of design, and the system's marketing depends on the semiconductor technology and system design techniques used.

1.3.2 Applications of Narrow-Band Receiver in Wi-MAX

Wi-Max, “Worldwide Interoperability for Microwave Access”, also familiar as IEEE 802.16, that is universally intended for the use of wireless metropolitan area networks (MAN). Wi-MAX is capable of providing broadband wire-less communication (BWA) up to thirty miles at some stations of the 802.16d standard, and around three miles for the mobile stations of 802.16e standard.

1.4 CMOS technology

Radio-frequency integrated circuit (RFIC) designs using Complementary Metal-Oxide Semiconductor (CMOS) technology are emerging strongly in the commercial world such as wireless LAN, Wi-MAX and Bluetooth. The core advantages of using CMOS technology for designing RF circuits is for the high speed, low cost, and CMOS technology allows for a high level of compact integration on a single chip. This is the main reason that CMOS is commonly used in very large scale integration (VLSI) technology where millions of transistors could be

integrated on a single die or chip. Another particular importance to RF designers is the high speed operating capability of CMOS. These advantages allow CMOS technology to operate effectively in the GHz frequency range with great levels of integration on a single chip while providing high performance and low cost. The current needs to exploit such regions of the radio spectrum, also modern digital telecommunications require high signaling rates, therefore makes CMOS a very useful technology choice.

1.5 Thesis organization

The thesis is organized into six chapters. Chapter 1 provides an introduction, motivation, objectives and an outline of the thesis. In Chapter 2, the RF receiver fundamentals including RFIC design parameters, receiver architectures are included. In chapter3 design trade-offs and conventional LNA Design topologies are described. In chapter 4, the basic cascade LNA model is discussed followed by chapter 5 where enhanced version of the cascade LNA is designed and the simulations are shown and then chapter 6 gives the Differential amplifier design based on the Enhancement techniques discussed in previous chapter followed by conclusion of thesis and suggests future works.

2. RF RECEIVER FUNDAMENTALS

2.1 Receiver architectures

The simple RF receiver architecture is shown in figure 2.1 as given in [2]. As Low Noise Amplifier is very first block in RF receiver Architecture, the performance of an LNA decides the overall performance of receiver. So, in this section, an analysis on two Rx designs is discussed, and also the key performance parameters for RF communication circuit design are discussed. After that an introduction to LNAs and trade-offs in LNA design is described. Next, the input matching architectures will be classified in LNA design and then examined. At the end, LNA load tuning techniques will be discussed.

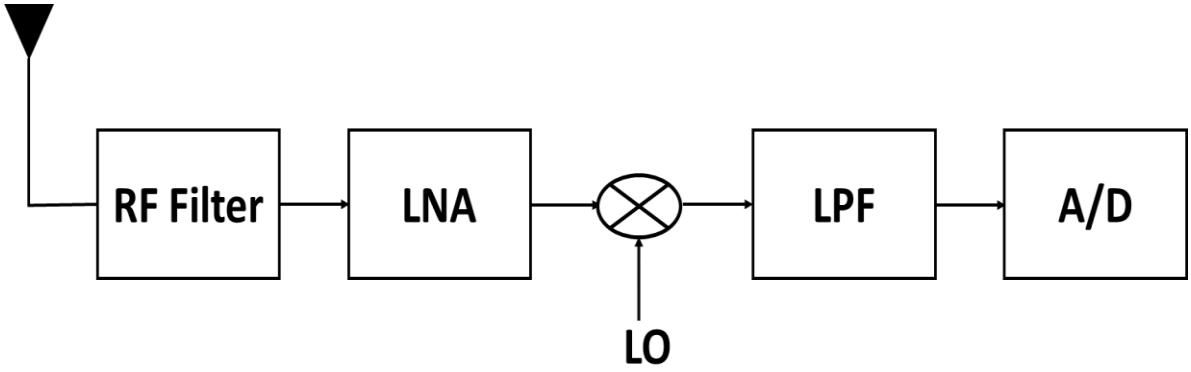


Fig 2.1: Block Diagram of RF receiver [2]

Complexity, design budget, power consumption, no. of outside modules are the main norms in the selection of receiver design. Here, two receiver architectures will be discussed which are: heterodyne receiver and homodyne receiver.

2.1.1 Heterodyne Receiver

The heterodyne receiver is perhaps the most widely used receiver architecture. Because of its reliable performance, it is widely implemented in many RF receiver applications. From Figure 2.2, as given in [2], incoming signal gets passed from the RF filter to lower the other frequencies i.e unwanted part of received signal. After being amplified from the Low Noise Amplifier, the signal gets filtered by the image reject (IR) filter to reduce the undesired signal's power level further. Next, the mixer down converts RF signal to the intermediate frequency (IF).

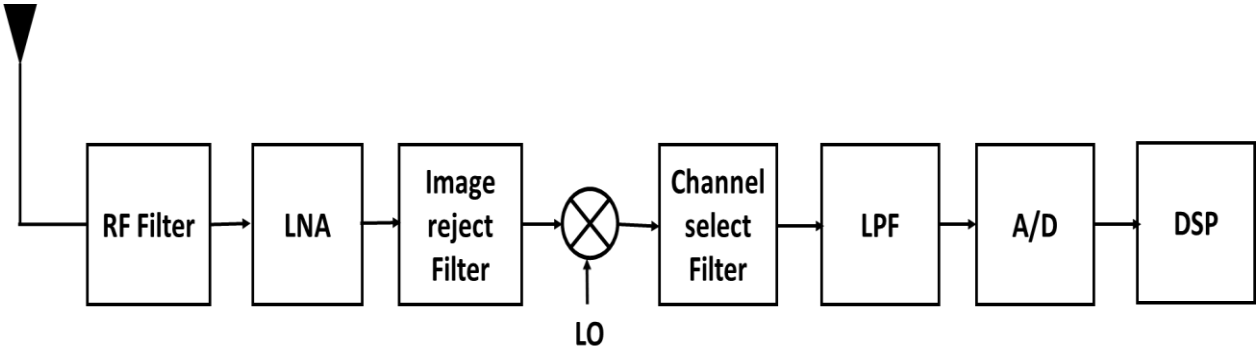


Fig 2.2: Heterodyne receiver architecture [1]

There are two types in mixer design: active and passive mixers. The active mixer uses DC power for providing active gain. The passive mixer does not consumes DC power but there is some conversion loss. To balance the lack of gain in the passive mixer, more gain is desired from the LNA stage. When signal passes through narrow-band IF filter, the signal gets converted to baseband signal and given to subsequent stages for further processing. Intermediate frequency is one of the main parameters in this receiver design. While choosing this IF value, we must look at the fundamental tradeoff between image rejection frequency and channel selection also between sensitivity and selectivity.

If we go for a higher IF, it eases image rejection because there image frequency gets further away from the desired frequency. The filter's quality factor is determined by angular resonate frequency. So a lower IF gives larger rejection of the interference from adjacent channels. Here it is shown in Figure 2.3, as given in [2] are the two cases corresponding to a high and low IF values to illustrate the trade-offs.

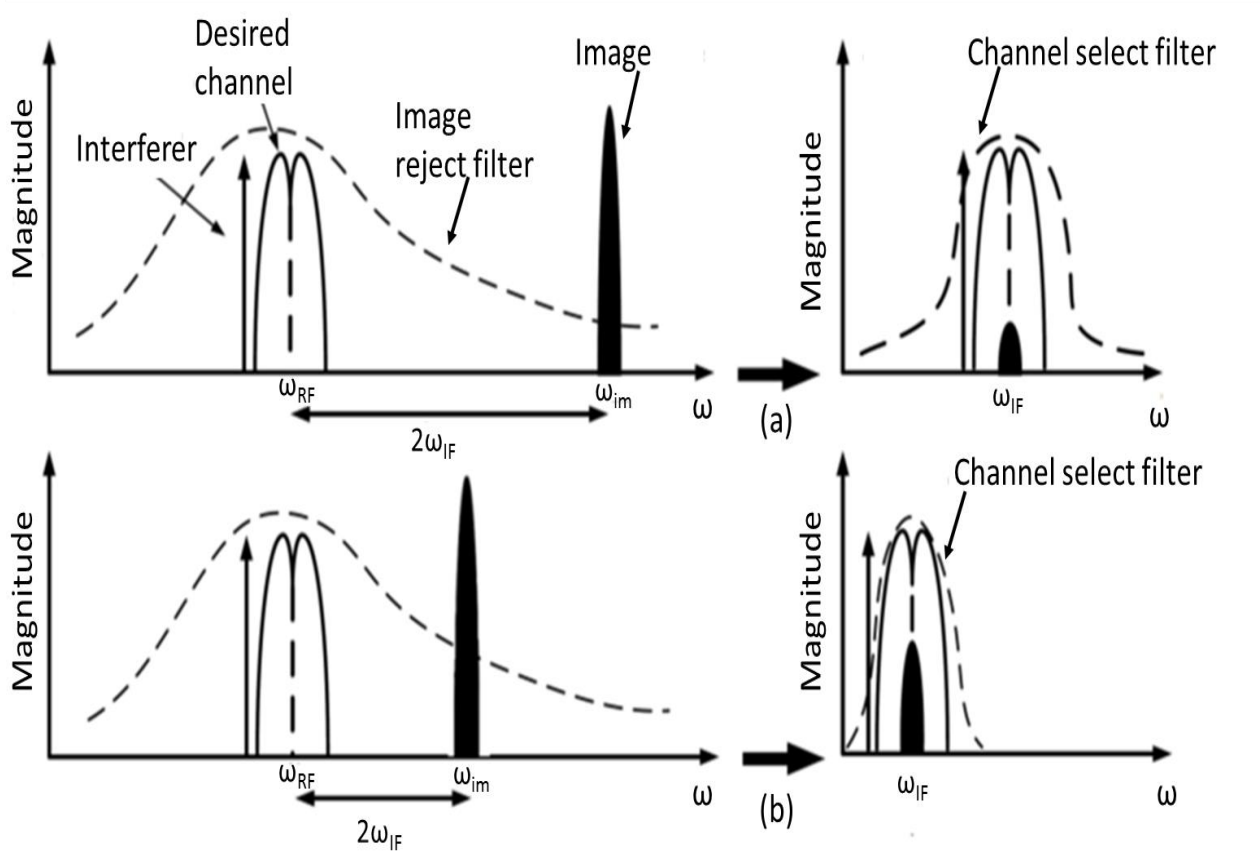


Fig 2.3: Image rejection versus lowering of interferers with (a) higher IF and (b) lower IF [1]

A higher IF leads to effective rejection of the image frequencies. However a low IF allows great suppression from nearby interferers. So, the choice of IF governed by the tradeoffs between the three parameters: image noise, space between the desired band and image occurrence, the loss from the image rejection filter. To lessen the images interference, we have to maximize IF or ready to with stand huge loss in filter for the increase of its quality factor.

2.1.2 Homodyne Receiver (Direct conversion receiver)

A homodyne receiver is also known as zero IF or direct conversion receiver. In double sideband amplitude modulated signals, down conversion is done with simple mixers. For the frequency and phase modulated signals, down conversion is performed with quadrature mixers to avoid loss of information because of positive and the negative part of the spectrum

overlap after down conversion. The block diagram of homodyne or a direct conversion receiver architecture is illustrated in Figure 2.4, as given in [2].

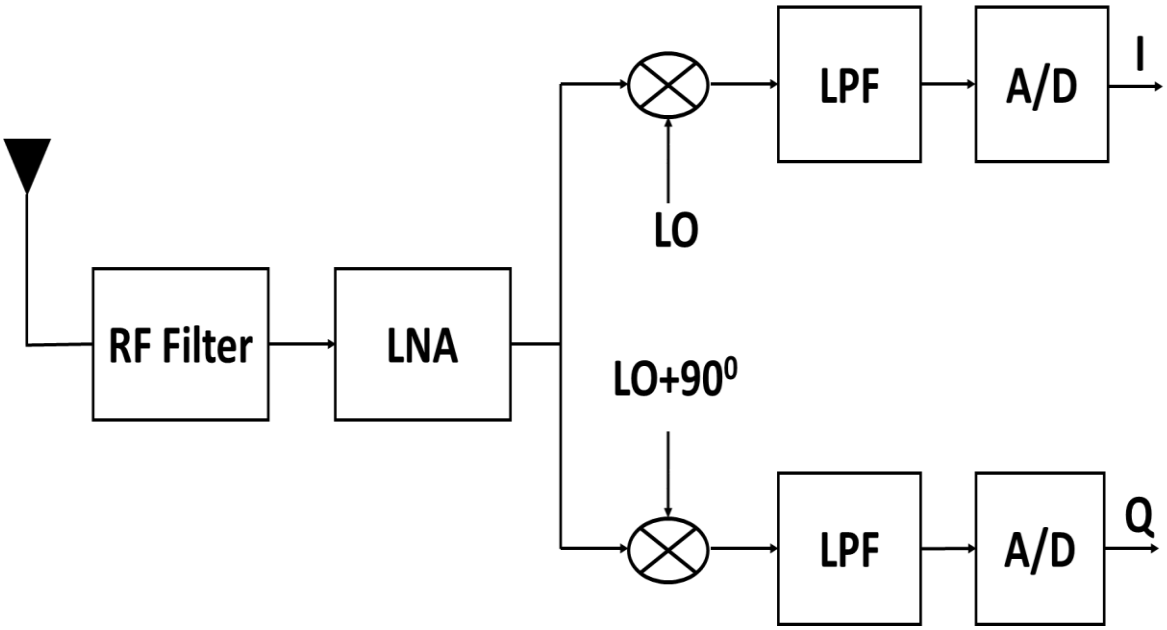


Fig 2.4: Homodyne receiver architecture [1]

A homodyne receiver structure is as similar as the low-IF receiver. The only difference is that it down converts RF signal frequencies straight to the base band frequencies. The simplicity of the homodyne architecture gives 2 more advantages than heterodyne receiver. First of all, the problem with the image frequency is eliminated because W_{IF} is equal to zero. So, we need not any IR filter in the design, and then LNA need not drive 50Ω impedance of IR filter, which can further reduces the overall power consumption. Secondarily, the IF filter and other subsequent down conversion stages will be substituted with LPF or the base band amplifier which makes useful in monolithic integration [19].

However, regardless of its simplicity, homodyne receiver has some other performance issues that obstruct its widespread usage [19]. DC offset problem is the main disadvantage in homodyne receiver. In homodyne topology, the IF frequency is base band frequency, any DC offset can be easily overwhelmed with the desired signal which saturates the following stages. There is no proper separation between local oscillator port, input of mixer stage and LNA. There is also a finite amount of feedback exists from LO port to LNA input and the mixer

input. Then this leakage signal is mixed with LO signal, generates a dc component. This process is called as “self-mixing”. A similar effect will be occurred if a large interferer gets leaked from LNA or mixer input to LO port and is multiplied by self [19]. Another problem of the homodyne receiver is I/Q mismatch. Because of the quadrature mixing requisite, here either RF signal of LO output needs to be shifted by 90^0. As shifting the RF signal usually causes severe noise, power and gain trade-offs, it is more reasonable to use topology shown in Figure 2.3. The I/Q amplitude mismatch and phase mismatch may cause degraded SNR performance.

2.2 Design parameters

2.2.1 Sensitivity

The RF receiver’s sensitivity quantifies the receiver’s ability to respond to a weak signal. Sensitivity is defined as the minimum detectable signal power level with no change in the specified SNR for analog receivers and bit error rate (BER) in digital receivers [19].

2.2.2 Noise figure

The performance of RF systems is generally limited by noise figure. Without noise, an RF receiver is able to detect arbitrarily small inputs and allows communication across long distances. This section, we reviewed some basic properties of noise and methods to calculate noise in the circuits. NF of LNA is directly added to the receiver output. In a typical RF receiver noise figure is generally 6 to 8 dB, it is estimated that the antenna or duplexer may contribute about 0.5 to 1.5 dB, then the LNA contributes about 2 to 3 dB, and the subsequent stages may contribute about 2.5 to 3dB. Even though, these values provide a good start in the receiver design, the exact value of the noise depends upon the performance of every individual stage in the receiver design. In modern RF electronics, we hardly design a LNA in isolation. Generally we design the RF receiver as one entity, and perform many iterations among the stages.

2.2.2.1 Noise as a Random Process

The main worry with the noise is that it is random. Engineers who are dealing with well defined, hard facts often find the randomness concept is difficult to understand, especially

if it needs to be incorporated mathematically. To get rid of this fear of randomness in noise, we approach this concept from an intuitive angle.

By means of "noise is random," we cannot predict the instantaneous value of the noise. For example, let us consider a resistor across a battery which carrying a current of V_B /R. Due to the temperature, each charge particle carrying the current experiences the thermal agitation, hence follows somewhat a random path while, on average, move towards the positive terminal of the battery. Thus, the average current remains equal to V_B/R. But the instantaneous value of current display random values.

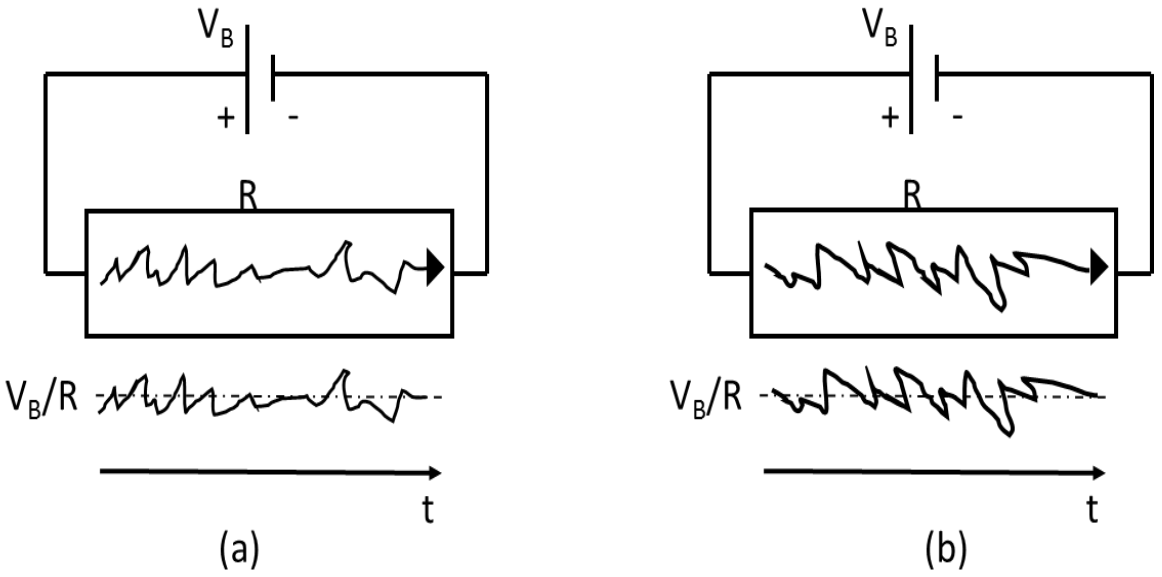


Fig 2.5: Noise as a random process [2]

Since noise cannot be described in terms of instantaneous voltages or currents, we look for other attributes of noise that can be predictable. For ex., we know that a higher temperatures leads to huge thermal agitation of electrons and creates larger fluctuations in the current Fig. 2.5(b), as given in [2]. To express the concept of random swings in a current or voltage quantity, we go for the average power of the noise, P_n written as below as given in [2]

$$P_n = \lim_{T \to \infty} \frac{1}{T} \int_0^T n^2(t)\,dt \qquad (2.1)$$

where n(t) is noise waveform as shown in Fig. 2.5, as given in [2]. The above definition simply means that we are computing the area under $n^2(t)$ for a long period, T, and normalizing the result to T, thus obtaining the average power of the noise. For ex., these two scenarios are depicted in Fig. 2.29 yields different average powers.

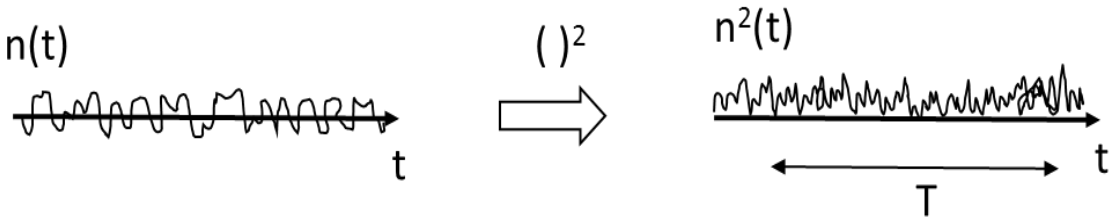


Fig 2.6: (a) Noise n(t) as a random process (b) squared noise $n^2(t)$ [2]

If n(t) is a random signal, how do we know about P_n? We are privileged that noise components in circuits have constant average power. For ex. P_n is known and constant for a resistor at a constant ambient temperature.

How to define the period? in Eq. (2.1). Because of its randomness, noise consists of variable frequencies. So, T must be taken long enough to accommodate as many cycles of the lowest frequency. For ex., the noise in crowded place arises from human voice which covers the range of 20 Hz to 20 kHz, needs the value of T be in the order of 0.5s to cover at least 10 cycles of the 20Hz components [2].

2.2.2.2 Noise spectrum

As we know, the time domain view of noise provides limited information, for e.g., the average power. On the other hand, frequency domain view yields greater insight and also more useful in RF design.

We may already have some understanding of the concept "spectrum." We say the spectrum of human voice ranges from 20 Hz to 20 kHz. This shows that if we can somehow measure the frequency content of the voice, we can observe all the frequency components from 20 Hz to 20 kHz. Then, how to measure a signal's frequency content, e.g., measure the strength of a component at 10 kHz. For this we need a filter out the remaining frequencies

from the spectrum and measure the average power at 10 kHz. For e.g., consider a microphone signal is applied to a band pass filter having a 1Hz bandwidth centered on 10 kHz. If a person speaks on a microphone at fixed volume, the power meter displays a constant value.

"Noise factor (F) is a measured from the noise performance of the circuit" [2]. It is often stated in decibels. Usually denoted as noise figure (NF).

$$NF = 10 \log F \tag{2.2}$$

Where F can be written as:

$$F = \frac{SNR(in)}{SNR(out)} \tag{2.3}$$

Where SNR(in), SNR(out) are SNRs measured at the input, output.

2.2.3 Harmonic distortion and Intermodulation

The linearity defines the highest acceptable signal level at the input of the system [2]. The Real life designs generally produces some amount of non-linearity. The Distortion in the Signal is a result of the non-linear conduct of the instances in the system. The widely used methods to find non linearity are: 1-dB compression point (P1dB), the third-order intercept point (IP3) [2].

2.2.3.1 The 1-dB compression point

"If a sinusoidal signal is applied at the input of a non-linear system, then the output generally produce some frequency components which are integer multiples of the applied input frequency" [2]. If the input signal is ($x(t) = Acoswt$) then output of the system will be:

$$Y(t) = \alpha_1 Acoswt + \alpha_2 A^2 coswt + \alpha_3 A^3 coswt + \ldots\ldots \tag{2.4}$$

Where α1, α2, α3… and so on are the corresponding Taylor series coefficient's of the applied sinusoidal at the input. A is amplitude of applied input (x (t)). In Eq. 2.4 the input frequency (w) is called fundamental frequency and its higher order frequency terms are called as harmonics. In many circuits, α_3 is less than zero [2].

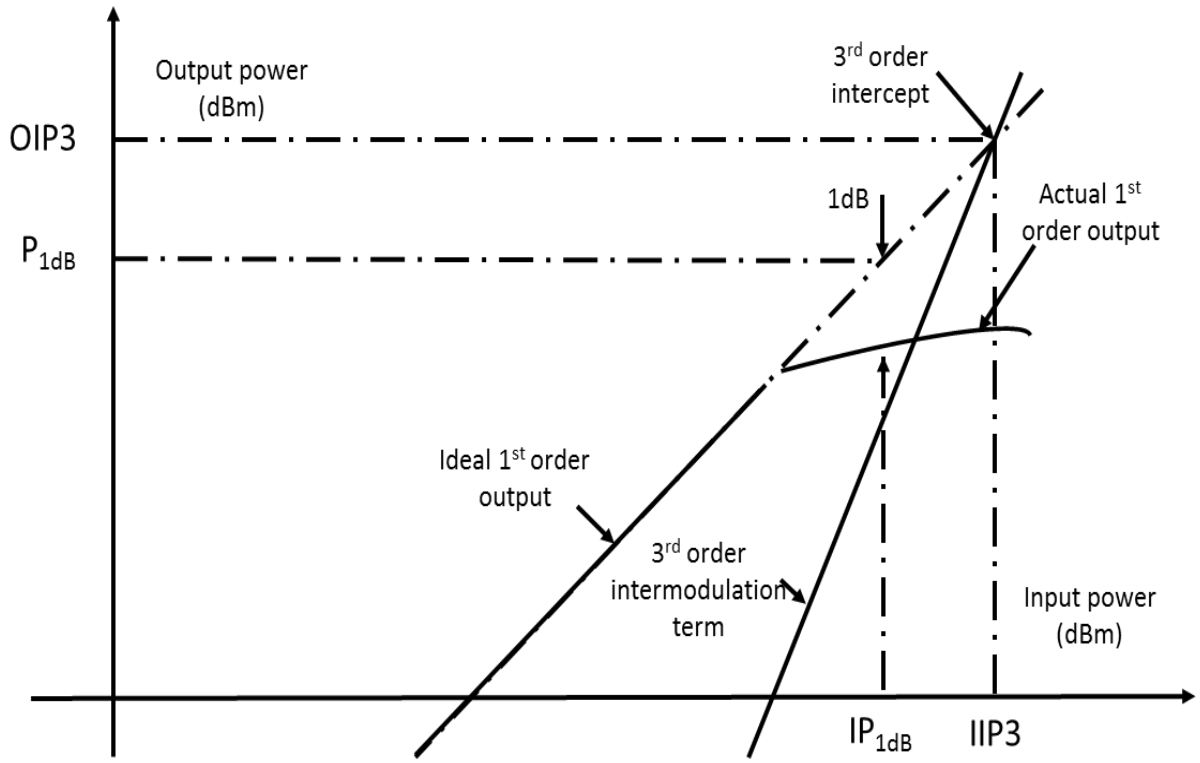


Fig 2.7: Illustrations of *P*1dB and *IP*3 (logarithmic scale) [2]

Hence, the gain of the system decreases with the amplitude A because of non-linearity. With the increase of input power, circuit gets into saturation and fundamental signal output misses to react linearly with input. The figure 2.7, as given in [2] shows the gain reduction due to the non-linearity of the system makes the power gain diverge from the supposed value. The point where the power gain comes down 1dB from the idealized value is taken as 1-dB compression point. At that input power level at which P1dB takes place is known as IP1dB. A system must be operated at some decibels lower than this P1dB value to evade non-linear region. 1-dB compression point is calculated as given in [2]

$$\text{IP1dB} = \sqrt{0.145\left|\frac{\alpha 1}{\alpha 3}\right|} \qquad (2.5)$$

2.2.3.2 The 3rd Order Intercept Point

While harmonic distortion is frequently used to describe nonlinearities in analog circuits, but in certain cases RF systems require other measures to know non-linearity behavior. One of the commonly used measure is the "third order intercept point" calculated from the two tone test [2].

When two signals are applied with different frequencies to the input of a non-linear system (Figure 2.8), as given in [1] then the output exhibits some undesired components which are not harmonics of the input frequency. Called as intermodulation. This phenomenon arises from the mixing (multiplication) of the two signals applied at the input. Let us assume the input signal as $x(t) = A1\cos\omega t + A2\cos\omega t$, then the output of the system will be:

$$Y(t) = \alpha_1 (A1\cos\omega t + A2\cos\omega t) + \alpha_2 (A1\cos\omega t + A2\cos\omega t)^2 + \alpha_3 A1\cos\omega t + A2\cos\omega t)^3 + \ldots\ldots \quad (2.6)$$

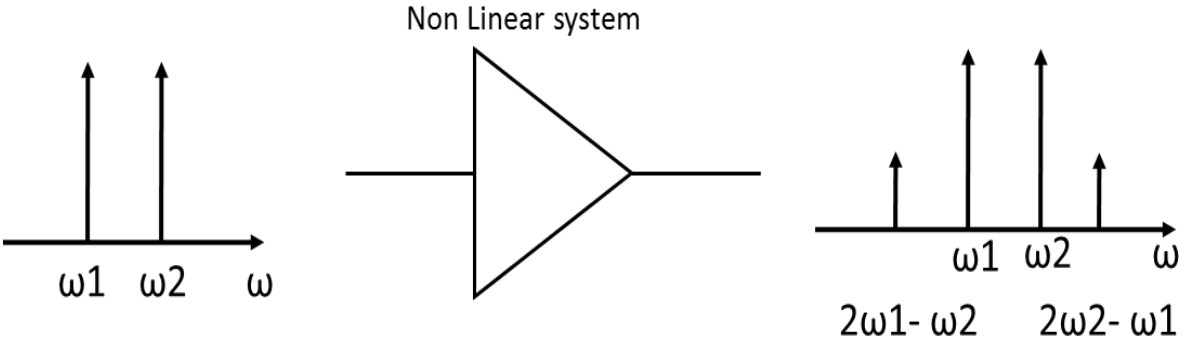


Fig 2.8: Intermodulation in nonlinear system [1]

As shown in Figure 2.8, if there is a small difference between W1 and *W2*, the third-order IM products at $2W1 \pm W2$ and $2W2 \pm W1$ may appear in the neighborhood of *W1* or *W2*, thus make nonlinearity. Intermodulation is also a troublesome effect in RF design. As illustrated in Figure 2.9, as gien in [1] if any weak signal is accompanied by two strong interferers, then system experiences third order non-linearity and one of the IM products falls in the band of interest, which corrupts the desired component.

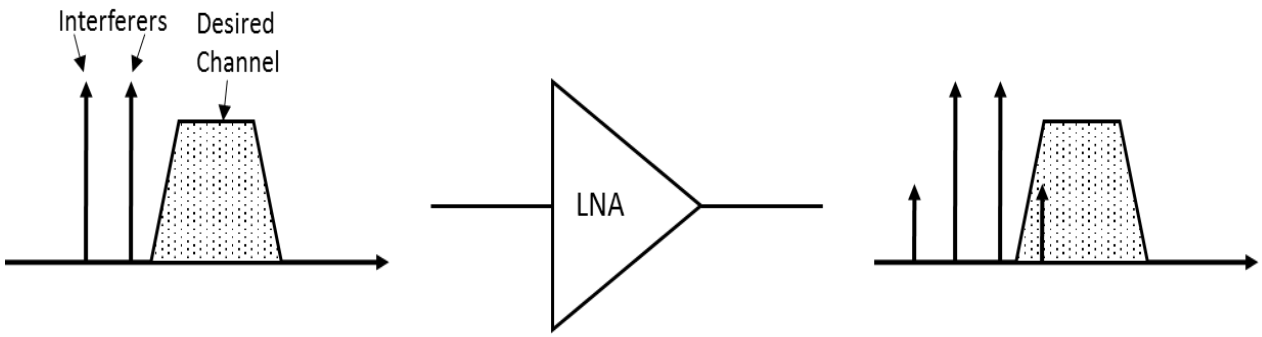


Fig 2.9: Corruption of a signal due to intermodulation between two interferers [1]

The "3rd intercept point" (IP3) is used to characterize the corruption of the desired signals due to third order intermodulation from two nearby interferers. It is measured with a 2 tone test where A1 = A2 =A. The input power at which the power level of the 3rd order IM product coincides with the fundamental is defined as 3rd order intercept point (IIP3) and the power level at the output called as "output 3rd order intercept point" (OIP3). IIP3 is calculated as given in [1]:

$$\text{IIP3} = 20 \log \sqrt{\frac{4}{3}\left|\frac{\alpha 1}{\alpha 3}\right|} \qquad (2.7)$$

2.2.4 S Parameters

There are different ways to describe the performance of a two port network (2PN). At lower frequency, parameters Y, Z, T and ABCD are frequently utilized. These parameters uses open and short circuit conditions to describe a linear electrical network behavior. But, these terminations are a bit difficult to realize at high frequency signals. In radio frequency (RF) range, scattering parameters (S-Parameters) is widely used to describe the network behavior. S-Parameters uses matched load termination and measurements are based on incident and reflected waves at the input and output ports. Figure 2.10 shows a two-port network as given in [3], where a_1 and a_2 are the incident waves, and b_1, b2 are the reflected waves. Their relation is expressed with S-Parameters as given in [3]

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} S11 & S12 \\ S21 & S22 \end{bmatrix} \begin{bmatrix} a1 \\ a2 \end{bmatrix} = [S] \begin{bmatrix} a1 \\ a2 \end{bmatrix} \qquad (2.8)$$

The matrix is **[S]** called as scattering matrix, where S_{11} is input reflection coefficient, S_{12} is reverse isolation coefficient, S21 represents the forward gain, and S22 is the output return loss coefficient. They are measured according to Figure2.11 as given in [3] and equations (2.9a) – (2.9d):

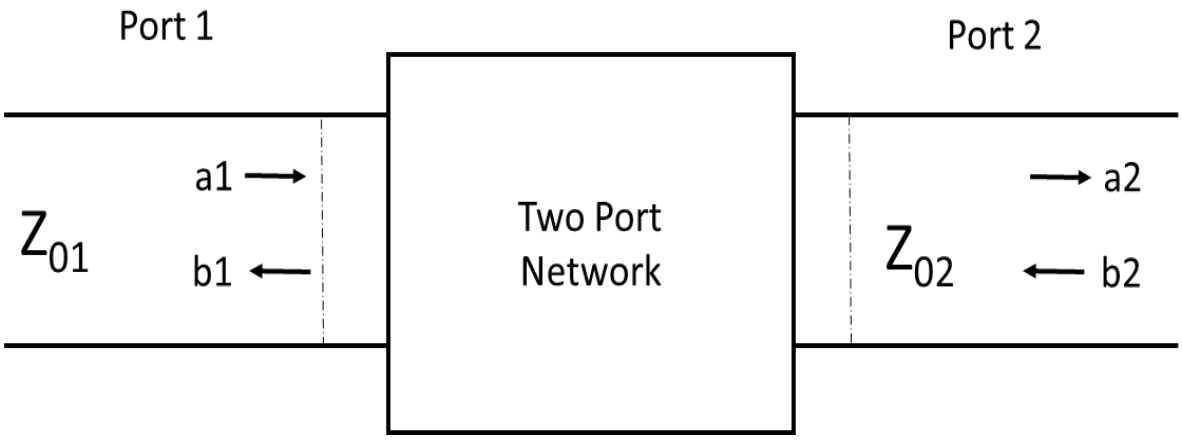


Fig 2.10: A Two Port network [2]

S11 = $\frac{b1}{a1}$ | a2=0 = input return loss coefficient with matched output port (2.9 a)

S12 = $\frac{b1}{a2}$ | a1=0 = reverse isolation coefficient with matched input port (2.9 b)

S21 = $\frac{b2}{a1}$ | a2=0 = forward gain coefficient with matched output port (2.9 c)

S11 = $\frac{b2}{a2}$ | a1=0 = output return loss coefficient with matched input port (2.9 d)

From the view point of the amplifier design, S_{11} and S_{22} represent how good the impedance at input and output are matched to source. S_{21} measures the amplifier's amplification gain. S_{12} represents the isolation from the output to input port. We can convert S-parameters to Y-parameters or any other network Parameters. Detailed formulae for the conversion can be found in most microwave textbooks, such as [3]

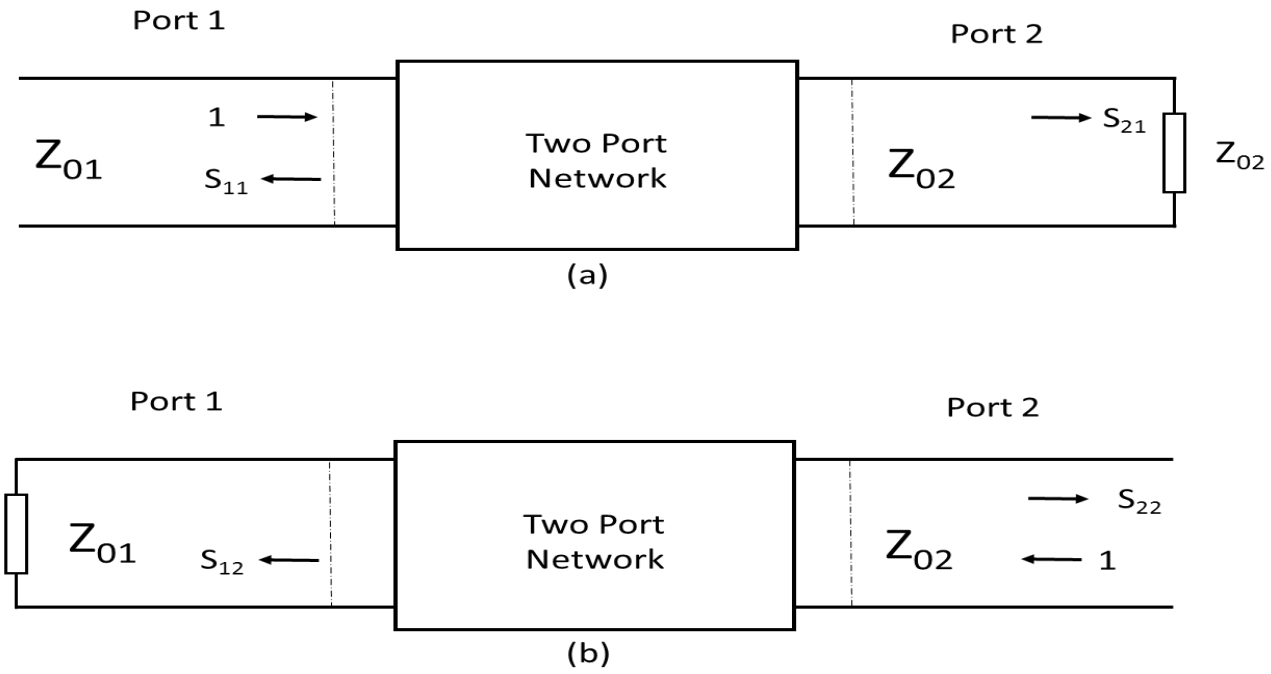


Fig 2.11: Measurement of S-parameters using (a) matched output port, (b) matched input port [3]

3. LOW NOISE AMPLIFIER

3.1 Introduction to LNA

Typical RF transceiver consists of simple receiver and transmitter path. In transmitter, only required signal exists. So transmitter path design become simpler, so many problems such as noise, selectivity and interference will be relaxed. The receiver path, the received RF signal is weak because of noise and interferers. LNA is first block in receiver.

In General, the incoming RF signal is considerably small (usually around -100dBm), which makes a small SNR at the output of RF system. Any extra noise in the subsequent stages will further degrade the SNR and therefore the receiver's performance. Since LNA is primary gain stage in receiver path, its NF should be low enough to keep the overall systems SNR high. Moreover, the gain of the LNA needs to stay high enough to further reduce the noise contribution from the succeeding mixer and all other stages, but not to be too high to worsen the overall systems linearity. The linearity of LNA is a critical parameter, except for some systems such as Code-Division Multiple Access (CDMA), where both receiver and transmitter are on at the same time.

In a conventional super-heterodyne receiver, As the RF filter and the image reject filter, are typically required to be matched to 50Ω impedance , will be placed in front of LNA and after the LNA, input and output impedance matching is part of LNA design specifications. Because of the removal of the image rejection filter, the output of LNA will be no longer matches with 50Ω impedance exactly. Hence, impedance at output needs to be optimized for a better performance of LNA and thence power consumption can be reduced by the elimination of the additional 50 Ω output driver stage that is normally required. Secondly, if we are aiming for full system integration, the LNA needs to provide the input matching with minimum number of discrete components. A fully integrated LNA is the finest option. Lastly, power dissipation is a concern, especially for the portable devices. In conclusion, the essential features in the design of LNA in these days receiver architecture are: Noise Figure, amplifier gain, input matching network, power consumption, reverse reflection coefficient, chip size and linearity (Figure 3.1) as given in [3]

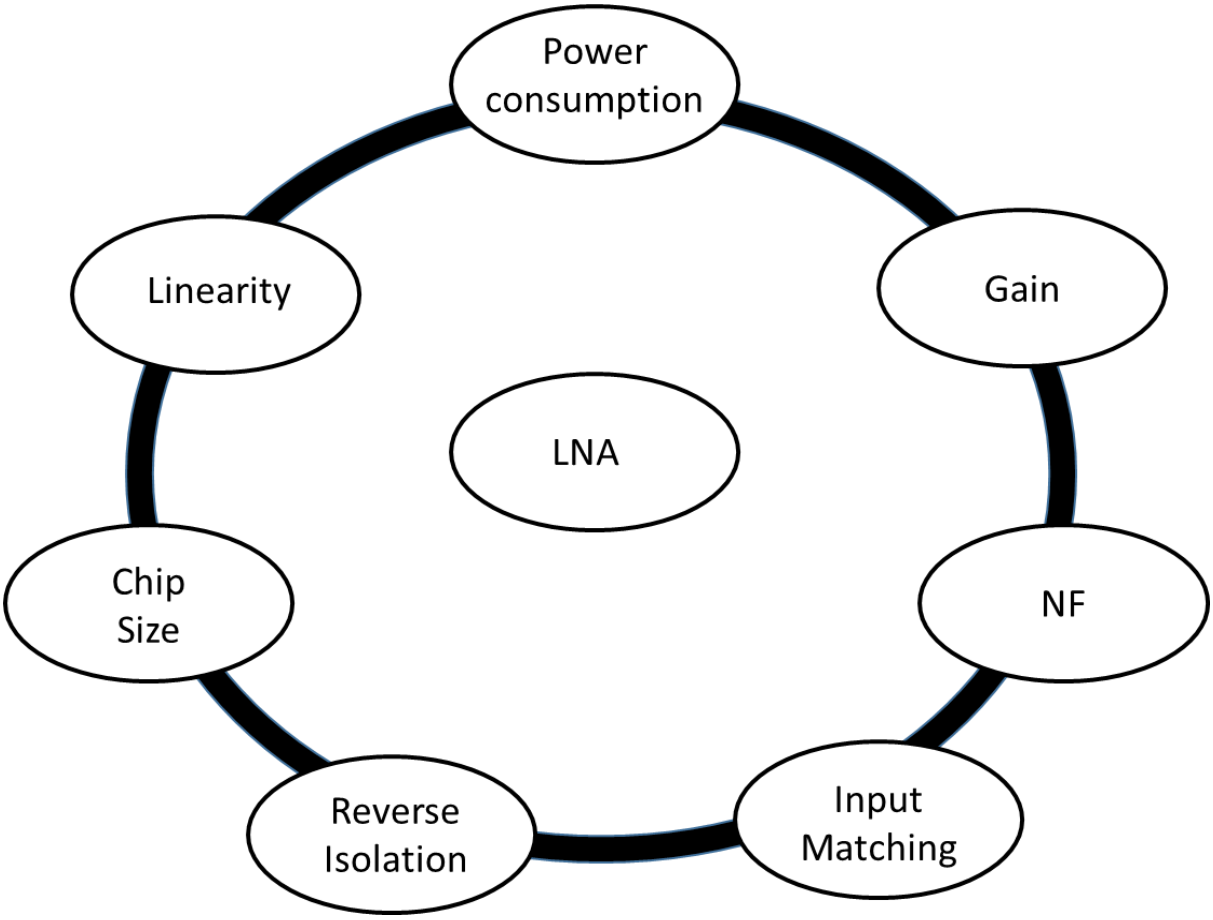


Fig 3.1: Important features in LNA design [3]

3.2 Performance trade-offs in LNA design

Different applications have different requirements for LNA performance. Hence, it is most useful if we could understand tradeoffs in the LNA design. Two important trade-offs are gain versus power efficiency and linearity versus current.

3.2.1 Gain vs Power efficiency

As we know, an amplifier's gain is generally proportional to the trans-conductance "g_m" *of* its input transistor. Higher g_m is desirable for higher gain. From the saturation region dc current equation 3.1 for long channels, we can write it as given in [1]

$$\text{Ids} = \frac{1}{2} K \frac{W}{L} (Vgs - Vt)^2 \qquad (3.1)$$

$$g_m = \sqrt{K\frac{W}{L}Ids} \tag{3.2}$$

$$\frac{gm}{Ids} = \frac{2}{(Vgs-Vt)} \tag{3.3}$$

where K is technology dependent constant, and W, L are width and length of transistor, I_{ds} is drain source dc current in the transistor, Vgs is the applied gate- source voltage and Vt is the threshold of the transistor. From equation (3.1) to (3.3), as given in [2] we can understand that Ids is directly related to $(Vgs - Vt)^2$, where (g_m / Ids) is inversely related to (Vgs -Vt). It's because the equation (3.3) is only applicable if the transistor is in saturation region. In sub threshold region, the MOSFET behave like a BJT, thus (g_m / Ids) is nearly a constant. The expression of (g_m / Ids) in sub-threshold region is written, as given in [2]

$$\frac{gm}{Ids} = \frac{1}{nVt} \tag{3.4}$$

where *n* is the sub threshold slope. In the 0.18 μm RF CMOS technology it is roughly equal to 1.0-1.5. The LNA analysis and simulations clearly determine the trade-off between gain and power efficiency. High gain but low power efficiency can be achieved with high Vgs. where high power efficiency but low gain can be achieved with low Vgs.

3.2.2 Linearity vs Current

Let us assume the nonlinearity of a MOS transistor arises from trans-conductance nonlinearity [2]. The IIP3of an LNA can be calculated as given in [2]:

$$\text{IIP3} = 20\log\sqrt{\frac{4}{3}\left|\frac{g1}{g3}\right|} \tag{3.5}$$

Where g1 and g3 are the 1st and 3rd order coefficient of M1's trans-conductance obtained by the derivative of drain to source dc current Ids with respect to the gate to source voltage Vgs at the dc bias point.

3.3 Gain

The gain of LNA must be as large as possible to reduce the noise contribution from subsequent stages in receiver, especially from the down conversion mixer(s). As described in Chapter 3.2, choice of the LNA gain leads to trade-off between the noise figure, linearity of receiver. As higher gain makes the nonlinearity of the subsequent stages more effective. In modern RF designs, the LNA directly drives the down conversion mixer(s) with no impedance matching between the LNA and the mixer. Hence, it is more important and simpler to perform chain calculations at the receiver end in terms of voltage gain rather than power gain of the LNA.

3.4 Input Matching

The receiving antenna and LNA are interfaced with an interesting issue. This is where analog engineers are differed from microwave engineers. LNA is considered as simple voltage amplifier, then one generally wants its input impedance to be ideally large. By noise perspective view, one uses a matching network before the LNA to minimize noise figure. By power perspective, conjugate matching is used between antennas, LNA. Preferable methods in RF LNA design is discussed below.

To answer this, following observations need to be made. (1) The band pass filter placed between the antenna and LNA is designed as a high frequency device and should be terminated by a typical 50Ω impedance. If there is any significant deviation of load impedance from 50Ω seen by the filter (i.e., the LNA input impedance deviates from 50Ω), then there may be a loss and ripple at pass band and stop band characteristics of the filter. (2) Even without such a filter, the receiver antenna is designed for a certain real impedance as load. If its load deviates from the preferred real impedance value or contains any imaginary value, then there is a loss of signal. (3) In general, the antenna signal from the transmitter must travel a significant distance before reaching the receiver. Therefore, poor matching at the receiver input leads to considerable reflection, an unwanted loss, and maybe some voltage attenuation. To overcome these problems, the LNA is often designed for 50Ω resistive input impedance. Since none of the concerns mentioned here apply to the other interfaces in the RX architecture (e.g., between

LNA and mixer or LO and mixer), subsequent stages are designed to maximize voltage swing rather than power transfer. Quality of the input match is often expressed with the term input return loss. It is the ratio of reflected power to incident power. Return loss for a source impedance of R_S is given as in [2]

$$\Gamma = \left| \frac{Z_{in} - R_s}{Z_{in} + R_s} \right|^2 \tag{3.6}$$

From the previous section, it is understood that one of the common goals in the LNA design is to match the input to 50Ω. Matching for the LNA can be done in four ways: (1) CS with resistive termination (2) CS with shunt feedback (3) CG LNA (4) CS with inductive source degeneration. These matching networks are implemented in both single ended and differential architectures.

3.4.1 CS amplifier with Resistive Termination

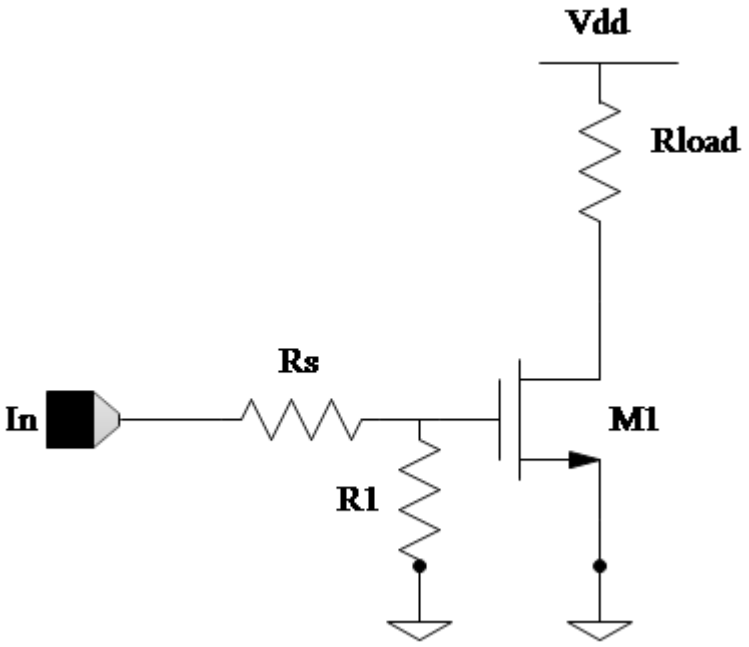


Fig 3.2: CS amplifier with resistive termination [2]

In this method, we use 50Ω resistor is used to provide 50Ω input impedance at the input port. A 50Ω resistor in parallel to input is used to design input matching for the LNA as

sown in Figure 3.2, as in [2] a. However, this resistive termination generates noise because of resistor. The noise factor [2] of this method can be calculated as:

$$NF = 1 + \frac{R_s}{R_1} + \frac{\gamma R_s}{g_m (R_s \parallel R_1)^2} + \frac{R_s}{g_m{}^2 (R_s \parallel R_1)^2 R_D} \qquad (3.7)$$

where γ is "excess noise coefficient" and gm is the trans conductance of the transistor. Even if R1 ≈ R_S, the noise figure exceeds 3dB. The NF of this structure is considerably high. This degradation is due to reason given below. The resistor *R*1 contributes almost equal noise as the source resistor *Rs* does. Which results in a factor of 2 in the first two terms of the equation (3.7), as in [2]. The higher NF makes this method unusual for the low noise amplifiers. So, good input matching network is desired. In the further techniques, LNA must be designed to provide a 50Ω input resistance without the thermal noise by a physical 50Ω resistor. This is possible with the use of active devices.

3.4.2 Common Gate LNA

The low impedance at the input of the common gate (CG) stage makes it useful for the LNA design. If channel length modulation and body effect are neglected, the impedance seen at the LNA input is $R_{in} = 1/g_m$. Thus, the dimensions and bias current of M1 are chosen so as to yield $g_m = 1/R_S = (50\Omega)^{-1}$.

Figure 3.3 shows the simplified circuit for CG-LNA as in [2]. The CG-LNA is widely used for wideband applications. The input impedance and voltage gain of a CG-LNA are:

$$Z_{in} = 1/ g_m \qquad (3.8)$$

$$A = g_m R_L \qquad (3.9)$$

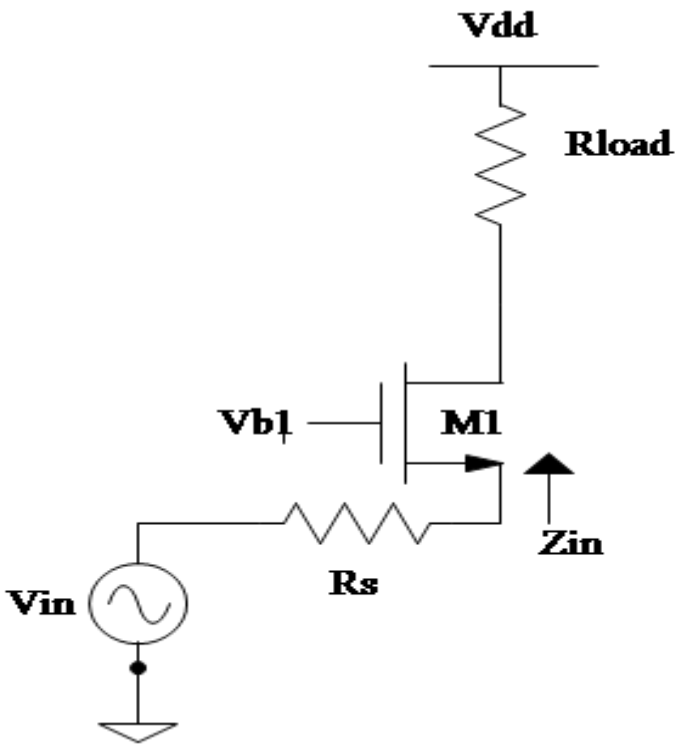


Fig 3.3: CG low noise amplifier [2]

To attain the input matching, the g_m value must be fixed at $1/R_S$. Thus, the load impedance R_L only remains as design variable. Because of this input matching limitation, the transistor's transconductance g_m should not be raised, hence makes a bound on noise figure LNA. Through derivations, total noise factor of CG LNA can be simplified as given in [2]:

$$NF = 1 + \frac{R_s}{R_1}\left(1 + \frac{1}{g_m R_s}\right) + \frac{\gamma}{g_m R_s} \tag{3.10}$$

$$NF = 1 + \frac{R_s}{R_1} 4 + \gamma \tag{3.11}$$

Even if $4R_S/R_1$ is smaller than $(1 + \gamma)$, the NF reaches 3 dB, because of the condition $g_m = 1/R_S$. i.e. a higher g_m yields a lower noise figure but also a lower input impedance. We know that the NF can be minimized, if some impedance mismatch is permitted at the input. Though, many other noises like the gate induced noise and the substrate noise will worsen the

performance significantly. Moreover, the load and the biasing circuits will generate extra noise. If we consider the effect of transistor's drain source resistance.

3.4.3 CS Stage with Shunt resistive Feedback

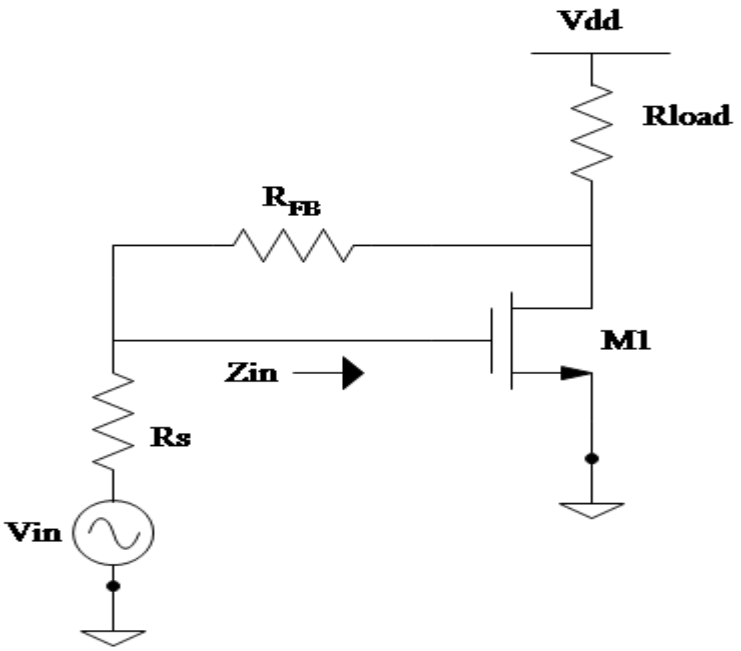


Fig 3.4: CS input stage with resistive shunt feedback [2]

Figure 3.4 shows another topology for impedance matching as in [2], which uses a resistive shunt feedback technique to set 50Ω match at the input. If the frequency of operation is lower than the f_T (unity gain frequency) of the transistor, the shunt feedback CS stage shown in Fig. 3.4 can be considered as a possible matching technique. Here, amplifier senses the output voltage and feeds a return current to the input. We go for this design technique for an input resistance equal to 50Ω and a reasonably low noise figure. The input impedance and noise figure can be expressed as in [2]:

$$Z_{in} = R_{fb} / (1+|A_v|) \tag{3.12}$$

$$NF = 1 + \frac{4R_F}{R_S\left(1-\frac{R_F}{R_S}\right)^2} + \frac{\gamma(g_{m1})(R_F+R_S)^2}{R_S\left(1-\frac{R_F}{R_S}\right)^2} \tag{3.13}$$

$$NF = 1 + \frac{4R_S}{R_F} + 2\gamma \tag{3.14}$$

For excess noise coefficient $\gamma \approx 1$, the NF exceeds 3dB even if $4R_S/R_F+2\gamma$ is much smaller than 1.

3.4.4 CS Stage with Source Inductive Degeneration LNA

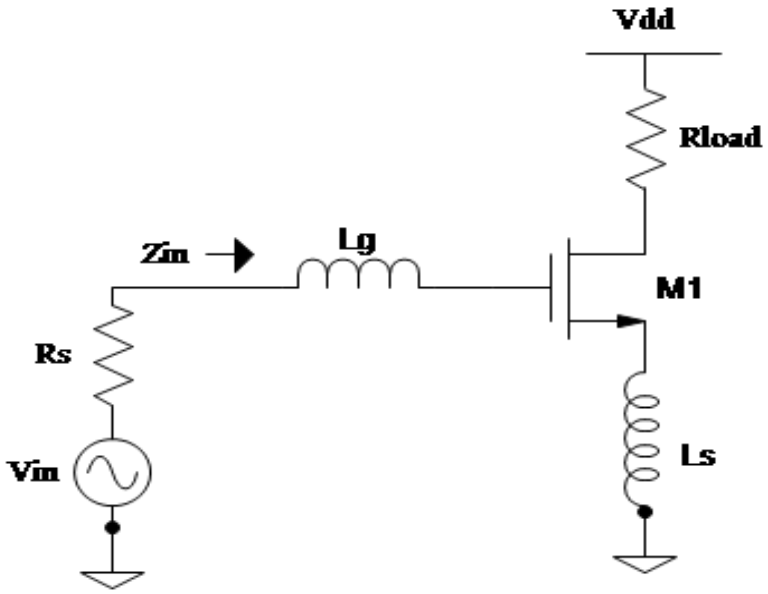


Fig 3.5: CS input stage with inductive source degeneration [2]

Figure 3.5 shows the fourth matching technique which uses source degeneration method to produce a resistive impedance through an inductor as in [2] without any usage of real resistor. The input impedance is given as in [2]

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{3.15}$$

From the equation 3.15, it is observed that there is a resistive term (g_mL_S/C_{gs}) in the input impedance that is directly proportional to degenerative inductance value. Whatsoever the value of resistive term is, it never generates thermal noise like an ordinary resistor, As we know that pure reactance is noiseless. Hence, this technique is preffered to provide the

required impedance without taking down the noise performance of the amplifier. For attaining a 50Ω impedance match at the input of LNA, the real part, of (3.15) equated to 50Ω and imaginary part of (3.15) must be zero at the design frequency. The resonance frequency is calculated as given in [2]:

$$\omega_0^2 = \frac{1}{(L_g + L_s)C_{gs}} \tag{3.16}$$

A detailed noise analysis and optimization of the LNA with this architecture are presented in [2]. The noise factor can be written as in [2]:

$$F = 1 + 2.4 \frac{\gamma}{\alpha} \frac{Wo}{Wt} \tag{3.17}$$

Where ($Wt = g_m / C_{gs}$) is the unity gain frequency. Based on the analysis in [2], the CS amplifier with source degeneration gives a low NF, significant gain and power consumption. Now a days, this topology is often used in the design of all narrow band LNAs. Though, LNA design, inductor Lg value has low quality factor, i.e., its parasitic resistance is considerably large, which will affect the matching and NF of LNA significantly. The input impedance calculated by taking the effect of parasitic resistance, r_L of inductor Lg into account, is given below as in [7]

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} + rl \tag{3.18}$$

The modified noise factor including r_L is given as in [7]

$$F = 1 + 2.4 \frac{\gamma}{\alpha} \frac{Wo}{Wt} + \frac{rl}{Rs} \tag{3.19}$$

3.5 Stability

Unlike the other stages in the receiver, the LNA must interface with the outside world. For example, if the user of a cell phone keeps his/her hand around the antenna, the antenna impedance changes [8]. For this reason, the LNA must be stable for all the source impedances at all the operating frequencies. We may think that the LNA must be operated properly only at the desired frequency band and not at other frequency band, but if LNA starts oscillating at any other frequency, LNA becomes extremely nonlinear and its gain will be compressed. A

parameter generally used to illustrate the stability of circuits is the "Stern stability factor," defined as in [2]

$$K = \frac{1 + |\Delta| - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \tag{3.20}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. If $K > 1$ & $\Delta < 1$, then the circuit becomes stable. In recent RF designs, the load impedance of the LNA is well controlled, which makes stability parameter K mistrustful. Since the LNA output is not matched to the mixer input impedance, S_{22} has become an ineffective quantity in such environment.

LNAs may be unstable because of ground and supply parasitic inductances formed by the packaging. For ex., if large series inductance is placed at the gate terminal of a transistor in CG configuration, the circuit may be suffered by a significant feedback from output to input. Also circuit become unstable at some frequency value. Hence, precautions should be taken in the circuit design and layout design while packaging.

3.6 Tuning techniques of LNA's Load

Besides the input matching network, the tuning techniques applied to the load at the device output will also affect the performance of the LNA. A good design of the tuning load aids in rejecting out of band frequencies and noise as well as to achieve a high gain. Three types of tuning loads commonly used are: resistive load, passive LC load and active inductor and passive capacitor load.

3.6.1 Ordinary Resistor as Load

An ordinary resistor can be used as the output load in LNA as in [1]. At times, resistor can be replaced by a MOS transistor. This method can be used in wideband output impedance matching and can be implemented with so ease. Though, it is not good for low noise applications, since the resistor generates thermal noise. Furthermore, the usage of resistive load reduces the voltage headroom for the transistor considerably. This results in a poor linearity if low supply voltages are used in the circuit.

3.6.2 Passive LC as Tuning Load

A tuned LC circuit can be used as the output load in LNA. It is the most widespread technique used in LNA designs as discussed in [1]. It is often used in communication systems to provide a selective amplification for the wanted signals and to remove the unwanted signals to certain extent.

4. CASCODE LNA AT 3.5GHZ

4.1 Introduction

Among the different LNA design types, the cascode LNA design is most widely used technique which is shown in Fig 4.1 as in [2]. This LNA improves the technical hitches of inductively degenerated CS LNA like progress in reverse isolation, Output matching network, noise figure etc. The inductively degenerated cascade LNA gives us

- Improved noise performance in the narrow band applications.
- Provides good isolation between the input and output.
- Ls and Lg are used to make impedence matching at the input.
- Output load matching can be obtained by proper tuning of the load inductor Ld and capacitor Cout.

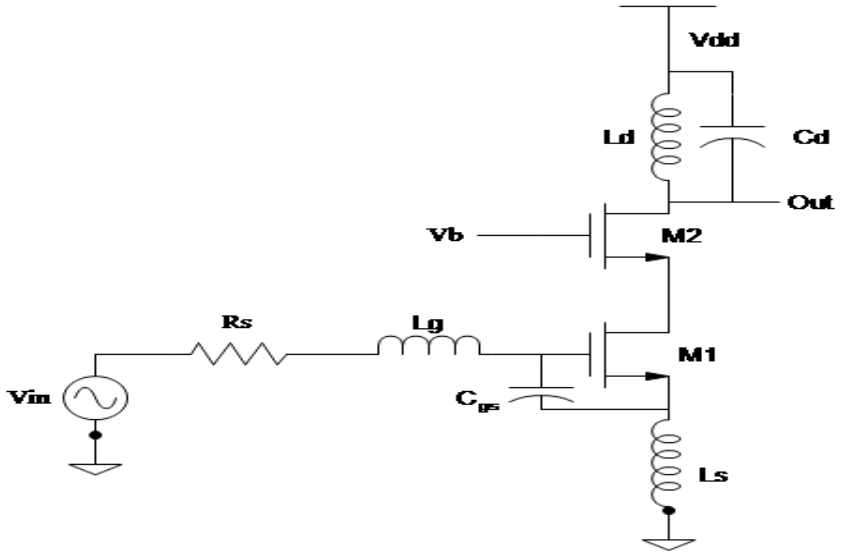


Fig 4.1: Architecture of Simple cascode LNA [1]

4.2 Principle of operation

The cascode LNA structure is the chosen structure because it can easily satisfy both noise and power gain requirements. The topology used here in this design is single ended cascode structure with inductive degeneration method for improved Noise Figure and input matching. By breaking down the gate width into smaller widths that are connected in parallel, the resistance at the gate terminal of input transistor can be reduced. This reduces gate resistance and increases the Cgs. The cascode structure provides higher output impedance and

reduces the Miller effect. An output grounded source buffer drives the load for proper output matching. The design is seen in Fig.4.2. The best matching to achieve desired Operating Gain, Noise Figure, and IIIP3 do not occur simultaneously. The Architecture of the 3.5 GHz LNA is shown in Fig. 4.2.

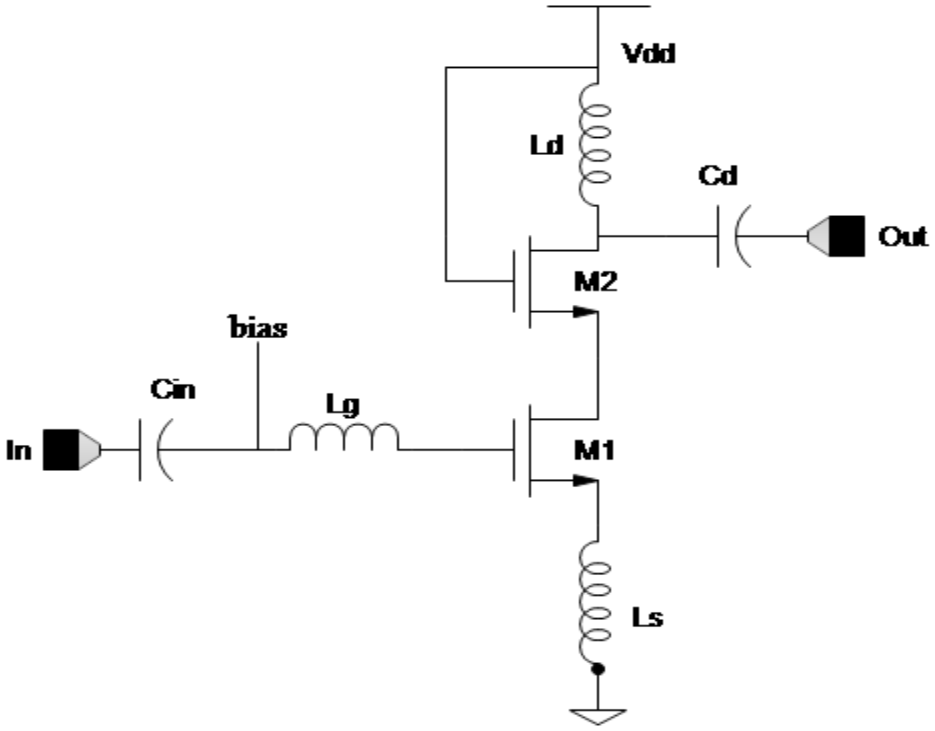


Fig 4.2: Schematic of Designed cascode LNA at 3.5GHz [1]

Source degeneration method is used to implement cascade LNA. Cascode transistor M2 helps to isolate the input from the output, it also decreases the gate-drain Cgd capacitance effect on LNA. Lg and Ls inductors are tuned to provide the input match. Usually Lg is varied to shift the circuit to desired operating frequency Ld and parasitic capacitances of M2 make a tank circuit at the load, which can be tuned to 3.5GHz. M3, Rbias1, Rbias2 provide biasing. M3 basically forms a current mirror with input transistor M1, transistor M3 width is chosen as a fraction of M1 width, so as to lower the power overhead from the biasing circuit. Capacitors Cin and Cout at input and output acts as DC blockers. Cin and Cout also play vital role in input and output matching respectively. As the choice of inductor and capacitor values are limited in technology using, matching network design turns to be very tough. The load inductor L_d is managed to overcome the tradeoff between forward gain, output matching, and power consumption, until input & output impedances are matched to 50Ω.

4.3 Design Approach

Having a good understanding of the cascode CS LNA of Fig. 4.1, here we describe a procedure for designing the circuit. The procedure starts with four knowns: the frequency of operation, ω_0, the value of the degeneration inductance, Ls, and the value of the input series inductance, Lg. Each of the last three variables is slightly flexible, but it is good to select some values to complete the design, and make iterations if necessary.

The design starts with the following two equations:

$$\omega_0^2 = \frac{1}{(L_g + L_s)C_{gs}} \tag{4.1}$$

$$R_S = \frac{g_m L_s}{C_{gs}} = 50\Omega \tag{4.2}$$

With ω_0 =3.5GHz known, C_{gs} is calculated from (4.1), and ω_T and gm (= $\omega_T C_{gs}$) from (4.2). Determine whether the transistor width can yield the necessary g_m and f_T simultaneously. In deep submicron technologies and for operation frequencies up to a few tens of gigahertz, the f_T is likely to be too high, but the pad capacitance alleviates the issue by transforming the input resistance to a lower value. If the requisite f_T is quite low, a capacitance can be added to C_{pad}. On the other hand, if the pad capacitance is so large as to demand a very high f_T, the degeneration inductance can be increased. In the next step, the dimensions of the cascode device is chosen often equal to the input transistor. As mentioned earlier, the width of the cascode device only weakly affects the performance.

The design procedure now continues with selecting a value for L_d such that it resonates at ω_0 with the drain bulk and drain gate capacitances of M2, the input capacitance of the next stage, and the inductor's own parasitic capacitance. If the parallel equivalent resistance of L_d results in a gain, greater than required, then an explicit resistor can be placed in parallel with L_d to lower the gain and widen the bandwidth. In the last step of the design, we must examine the input match. Due to the Miller multiplication of $C_{gd.}$ it is possible that the real and imaginary parts depart from their ideal values, necessitating some adjustment in L_g.

The foregoing procedure typically leads to a design with a relatively low noise figure, around 2 dB depending on how large L_g can be without displaying excessive parasitic capacitances. Alternatively, the design procedure can begin with known values for NF and Ls and the following equation:

$$NF = 1 + g_m R_S \gamma \left(\frac{\omega_0}{\omega_T} \right)^2 \tag{4.3}$$

where the noise of the cascode transistor M2 and the load is neglected. The necessary values of ω_T and gm can thus be computed ($gm_1/C_{GS1} \approx \omega_T$). If the device f_T is too high, then additional capacitance can be placed in parallel with CGS. Finally, LG is obtained from Eq. (4.3). (If advanced packaging minimizes inductances, then L1 can be integrated on the chip and assume a small value.)

The overall LNA appears as shown in Fig. 4.2, where the antenna is capacitively tied to the receiver to isolate the LNA bias from external connections. The bias current of M1 is established by MB and R1, and resistor R2 and capacitor Cin isolate the signal path from the noise of R1 and MB. The source bulk capacitance of M1 and the capacitance of the pad at the source of M1 may slightly alter the input impedance and must be included in simulations.

By breaking down the gate width into smaller widths that are connected in parallel, the resistance at the gate terminal of input transistor can be reduced. The input impedance, considering the parasitic resistance rL of inductor Lg, as in [10] is:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} + r_L \tag{4.4}$$

So, the minimum Noise factor is changed to:

$$F_{\min} = 1 + 2.4 \frac{\gamma}{\alpha} \frac{\omega_0}{\omega_t} + \frac{r_L}{R_s} \tag{4.5}$$

4.4 Simulation Results

The simulation results of cascode LNA shown in Figure 4.3, are shown in Figure 4.4 to 4.10. The designed LNA requires a 1.8V supply voltage and consumes a power of 9.81 mw. At 3.5 GHz, LNA has NF of 2.749 dB, with input return loss of -25.53dB, output return loss of -9.033dB, forward gain of 20.15dB. IIP3 of -11.9093dBm and has 1dB compression point at -17.8695dBm.

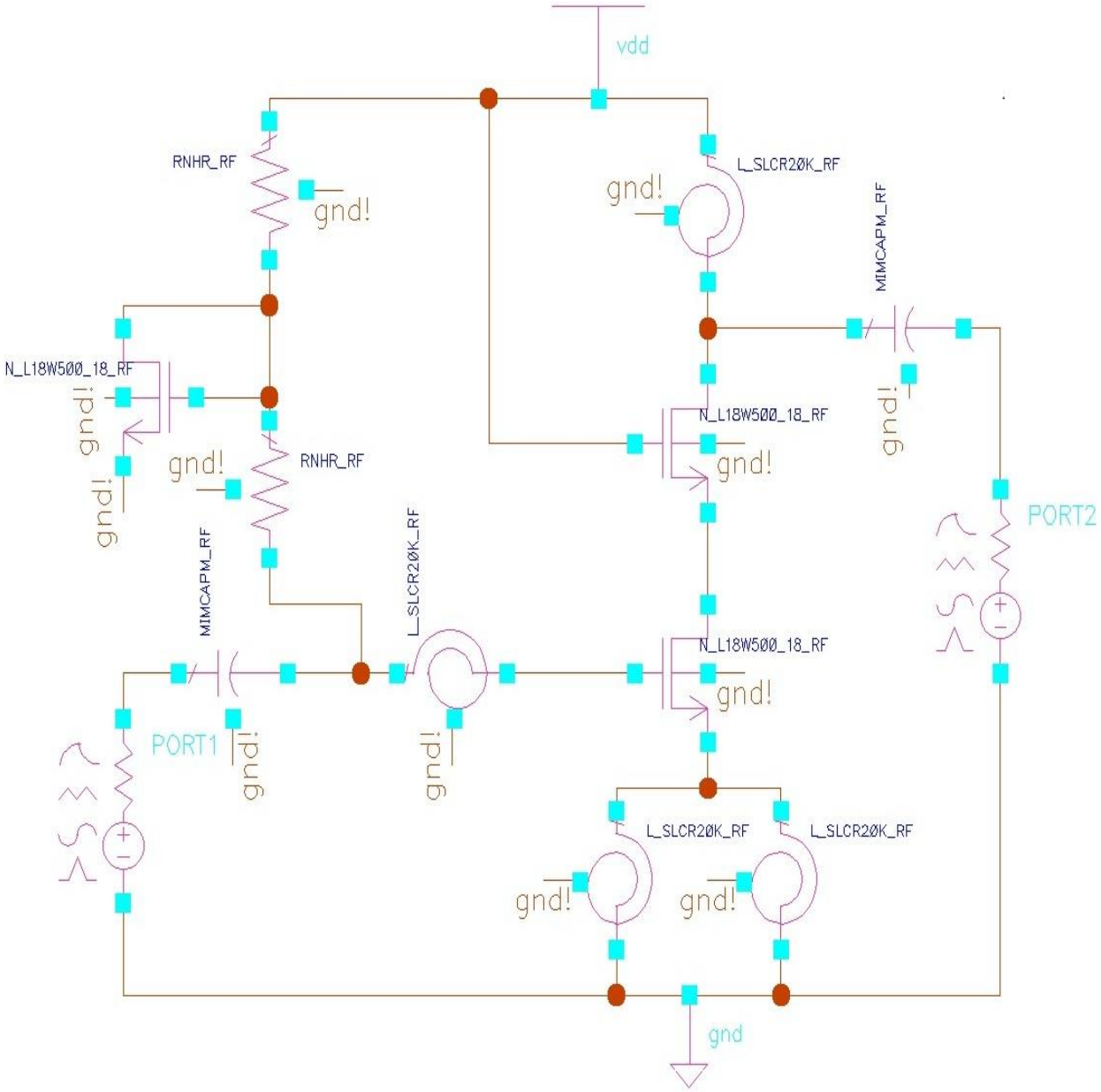


Fig 4.3: Schematic of CMOS CASCODE LNA at 3.5GHz

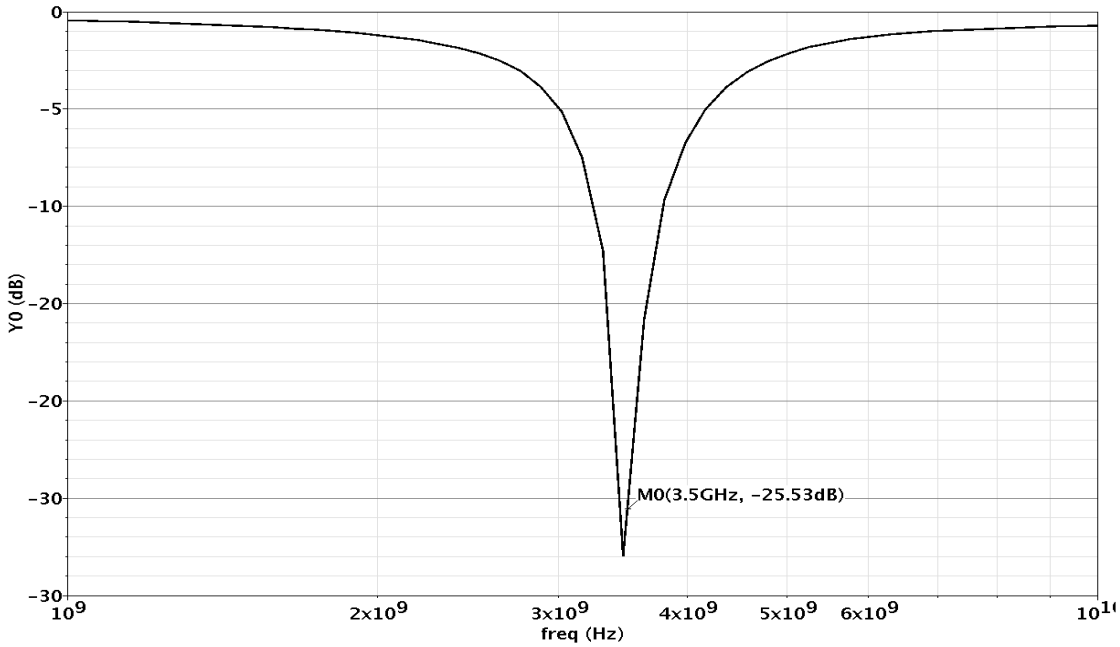


Fig 4.4: Simulation of Input Matching Parameter S11

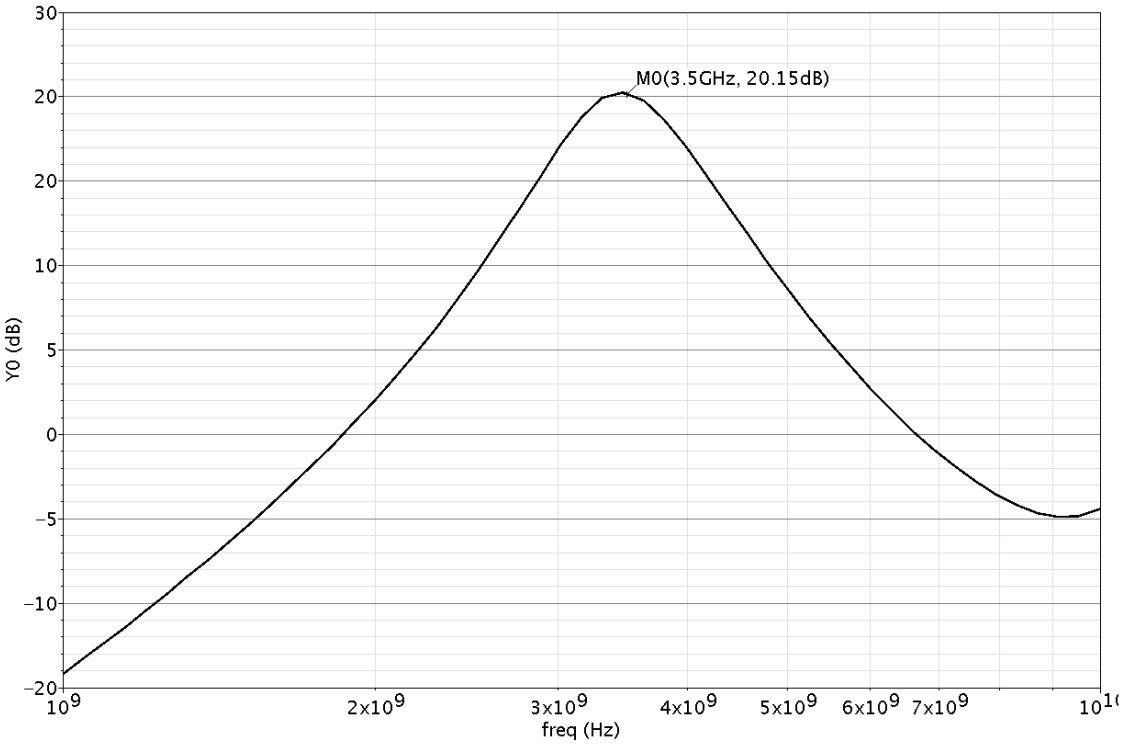


Fig 4.5: Simulation of Forward Gain Parameter S21

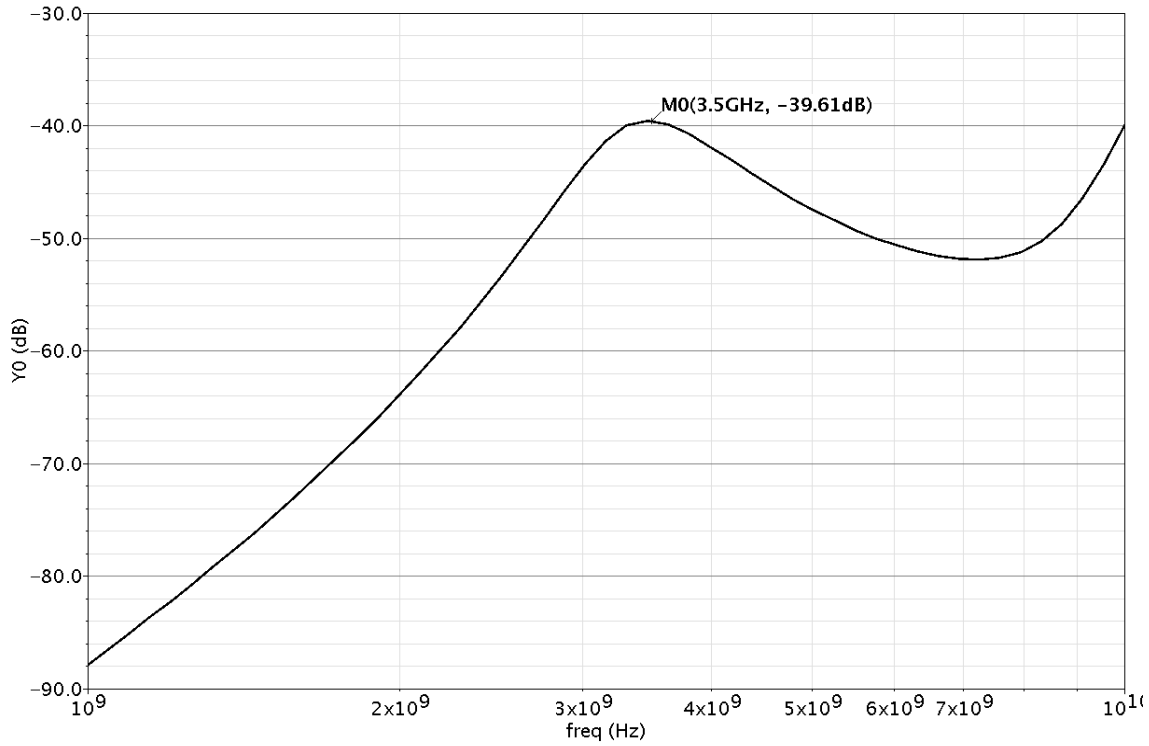


Fig 4.6: Simulation of Reverse Isolation Parameter S12

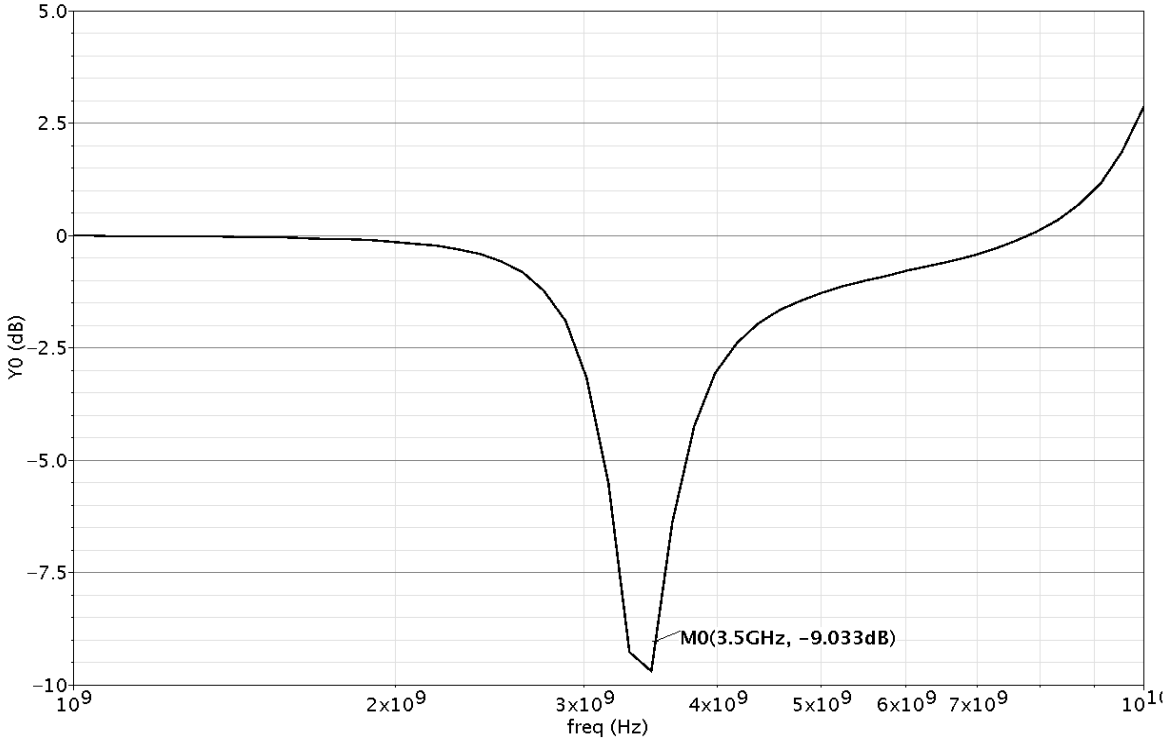


Fig 4.7: Simulation of Output Matching Parameter S22

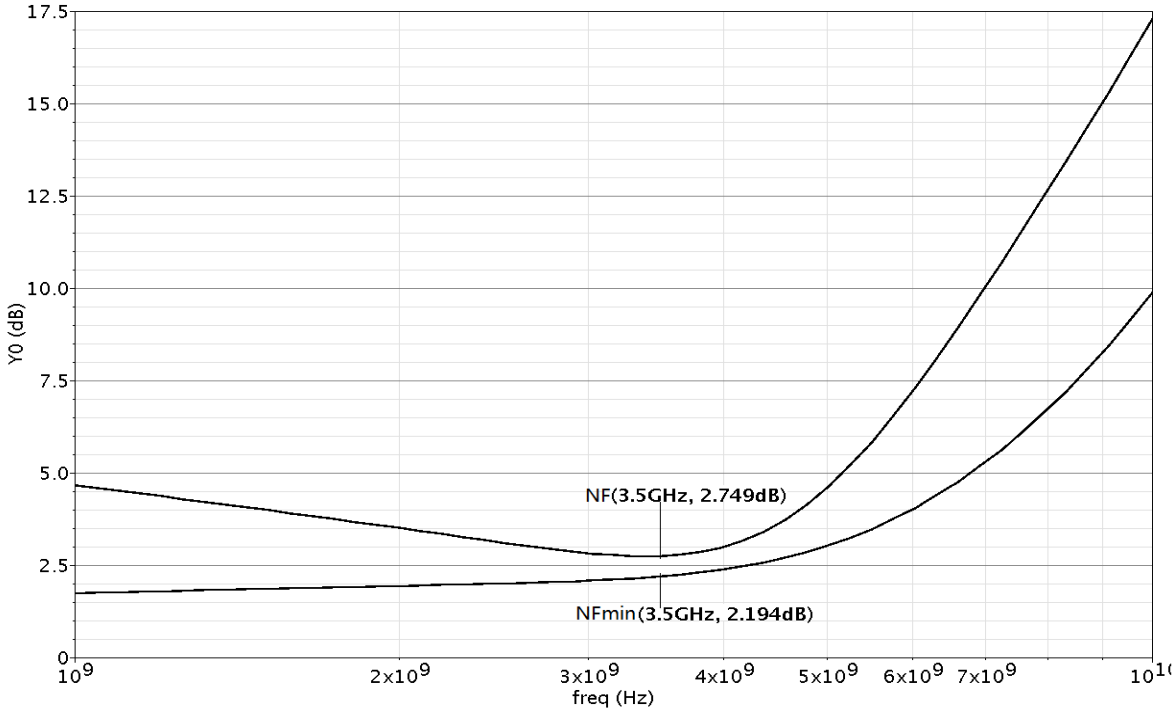


Fig 4.8: Simulation of Noise Figure & Noise Figure (min)

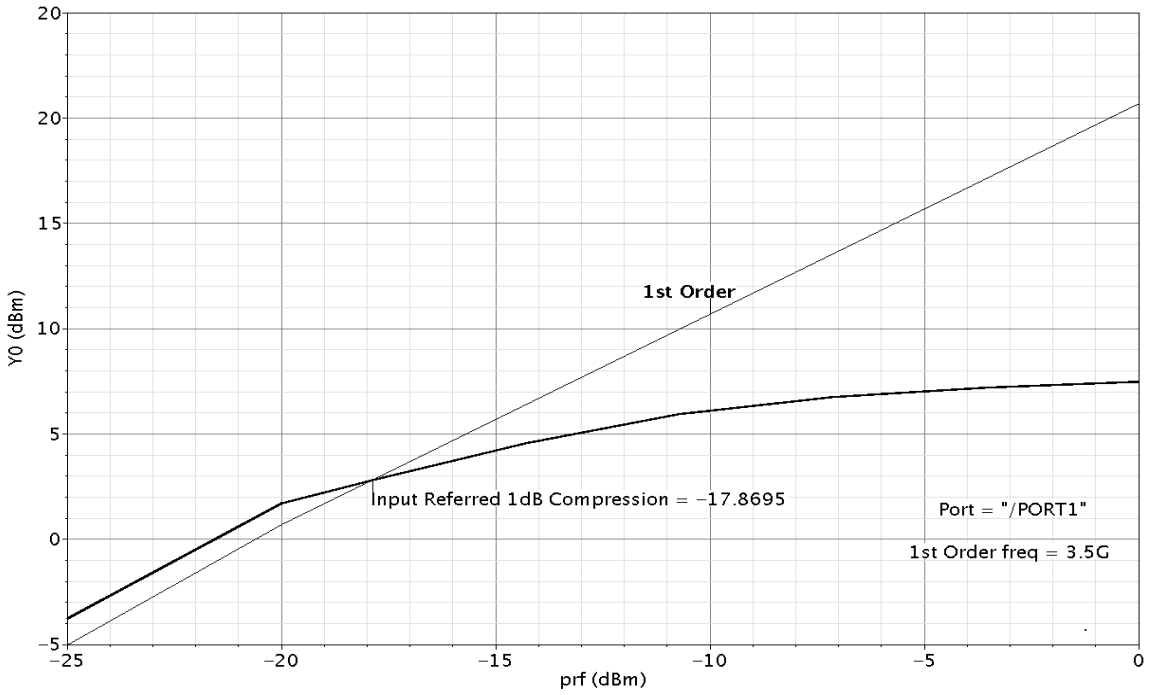


Fig 4.9: Simulation of 1dB Compression Point

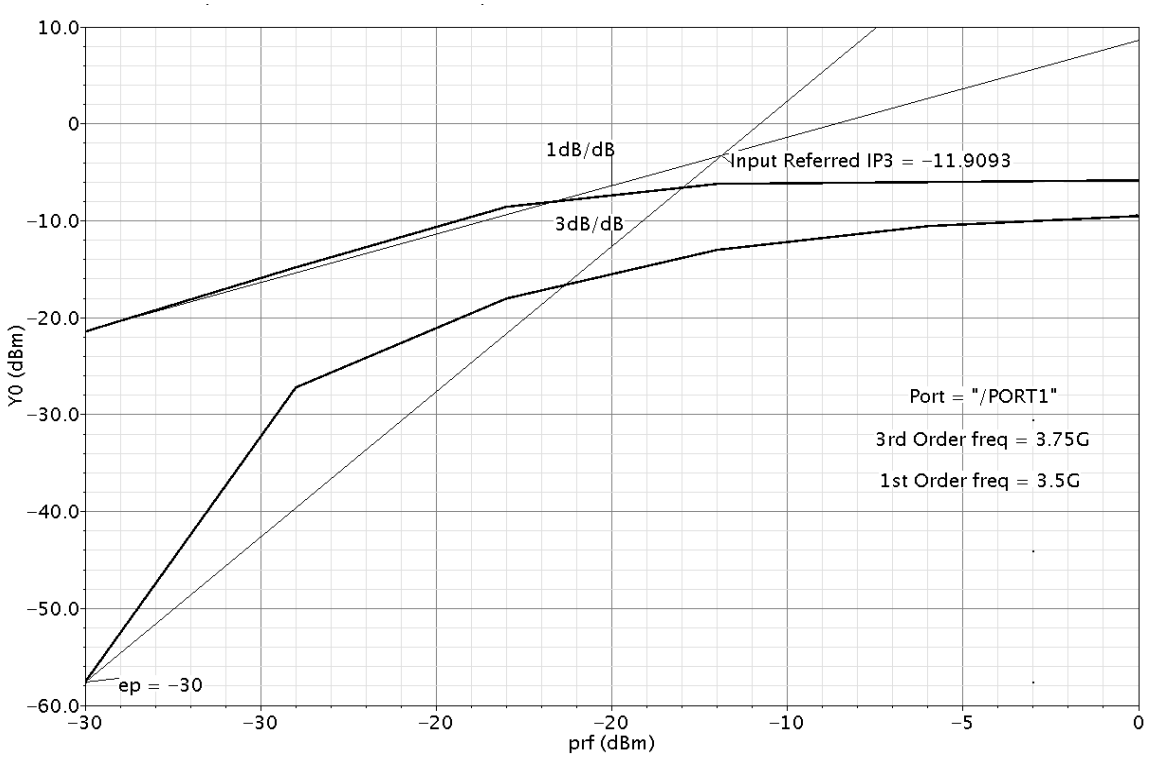


Fig 4.10: Simulation of Intermodulation Distortion IIP3

Table 4.1: Simulation of simulation Results for simple cascode LNA

PARAMETER	VALUE
S11	-25.53dB
S12	-39.61 dB
S21	20.15 dB
S22	-9.033 dB
NF	2.749 dB
NF(min)	2.194 dB
1dB compression	-17.8695 dBm
IIP3	-11.9093 dBm
Power consumption	9.8mw

This chapter presents a 3.5 GHz LNA design using UMC 0.18μm CMOS process, The LNA design requires only a 1.8V supply voltage and consumes 9.8 mw power, at 3.5GHz, this LNA has noise figure (NF) of 2.749dB, with input return loss of -25.53dB, output return loss of -9.033dB, and Forward gain of 20.15dB. This LNA performance represents good gain, with acceptable NF, and low power consumption. 1dB compression point of this design is -17.86dBm, means no gain compression for the received signals below compression point level. A two tone test is done to this LNA to observe the intermodulation, observed IIP3 is -11.9093dBm. The performance summary is listed in Table 4.1.

5. ENHANCED LNA AT 3.5GHZ

5.1 Principle of operation

The cascode LNA is the most preferred design among LNAs. Because it can provide low noise along with better gain at a time. Still, this Cascode topology suffers from the noise contributed by parasitic capacitances of transistors M1 and M2 [8]. Also we find difficulty in match and tune the load concurrently with the limited inductor and capacitor values

To minimise this noise, a series resonance inductor[8] is placed in between CS - CG stages as shown in figure 5.1, thus at that particular node, inductor removes the parasitic capacitance at the given frequency. Same concept is used at gate of the transistor M2.

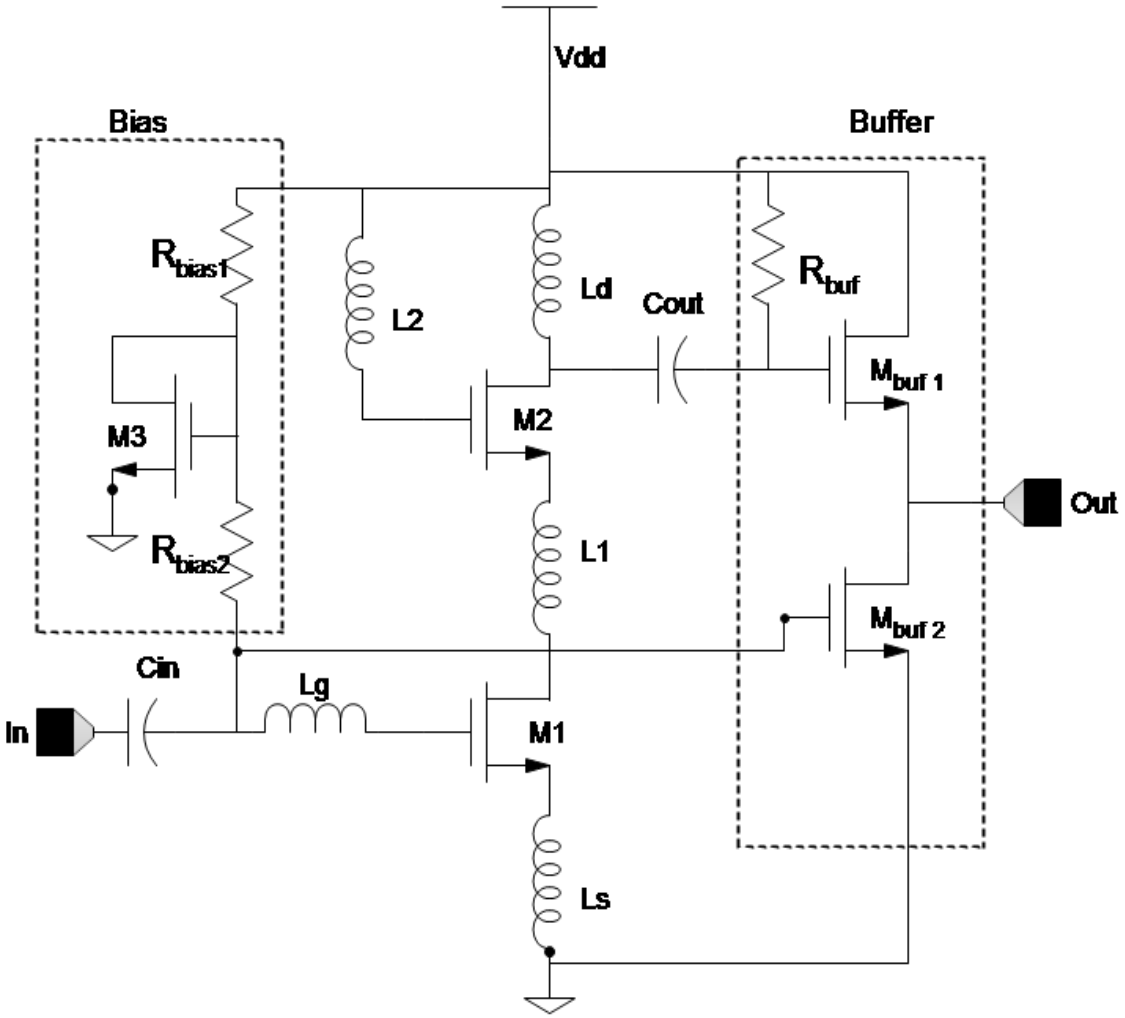


Fig. 5.1 Enhanced Architecture of cascade CMOS LNA

With these simple modification, we can observe the improvement in Noise figure and forward gain. This architecture shown in Fig. 5.1 can nullify parasitic effects at some value of inductor Lm at the operating frequency. The instances Lg and Ls are tuned to provide the input match. M3, Rbias1 and Rbias2 makes a current mirror with the input transistor and biasing. Cin and Cout are acting as DC blockers. Transistors Mbuf1, Mbuf2 along with Rbuf forms buffer stage, which is used to drive loads like mixer. This extra stage helps to achieve tuning and output matching parallelly. It is observed that this modified cascode LNA provides improved gain, NF and output match.

5.2 Simulation Results

The designed LNA at 3.5GHz, shown in Fig. 5.1, was simulated using the cadence 0.18µmc RF spectre tool. Schematic and layout diagrams are shown in Fig 5.2 and 5.3 respectively. Pre and post layout Simulation results are shown in 5.4 -5.17. From the following simulation results, we can observe a small difference between pre and post layout curves, because of parasitics formed during the layout process.

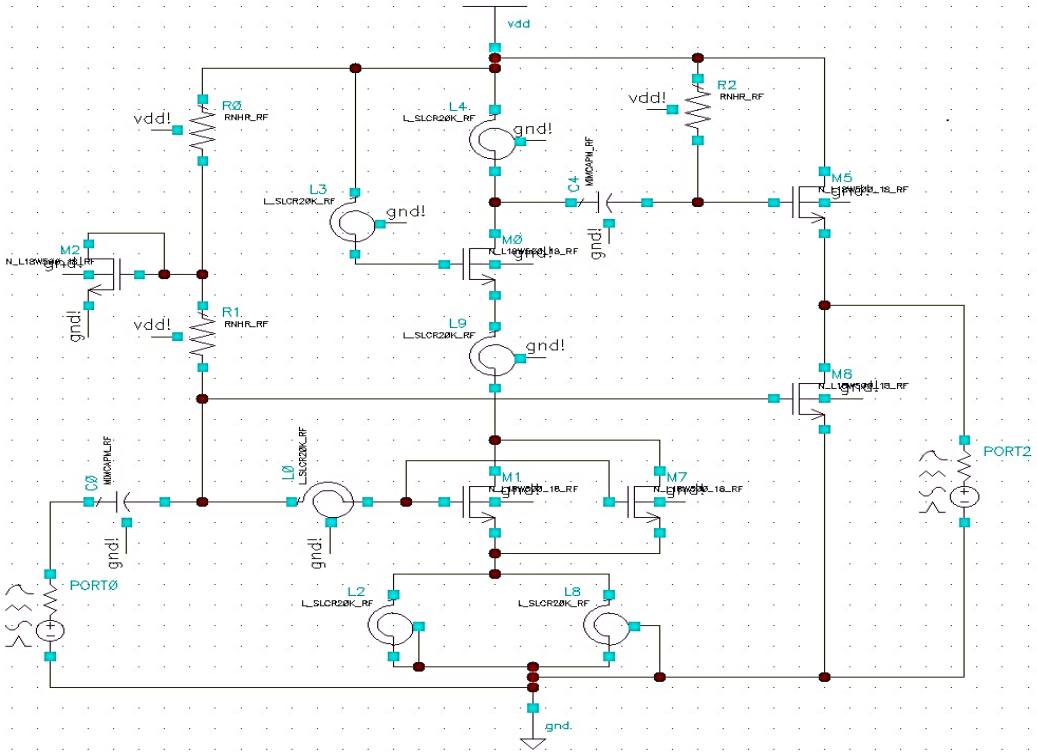


Fig 5.2: Schematic of proposed cascode LNA at 3.5GHz

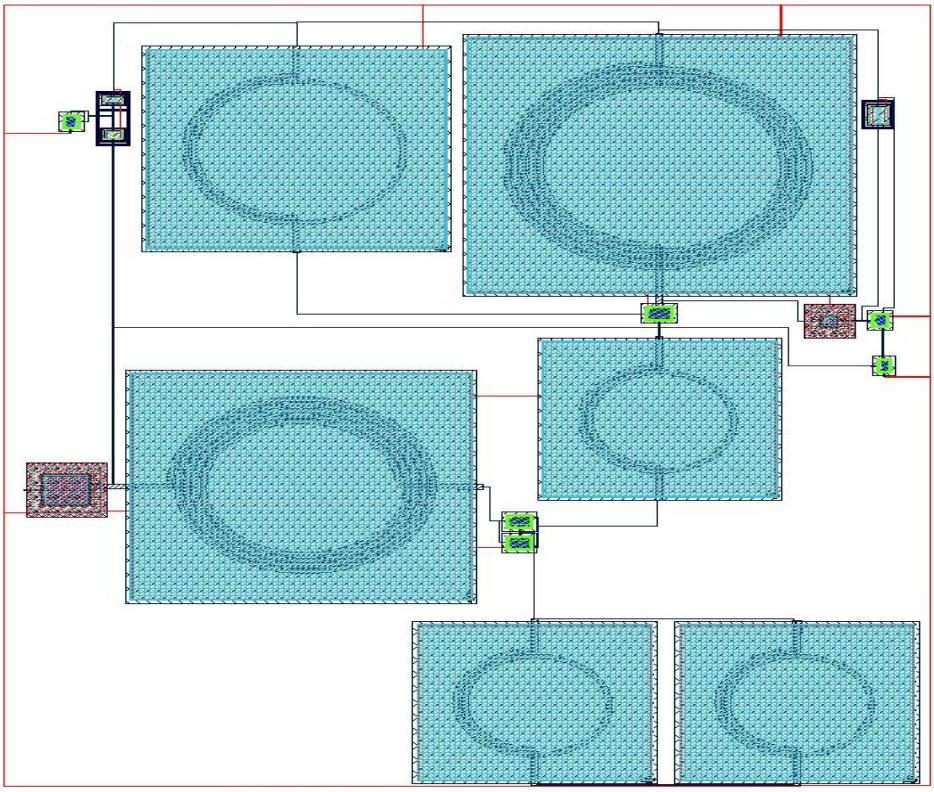


Fig. 5.3: Layout of the proposed LNA

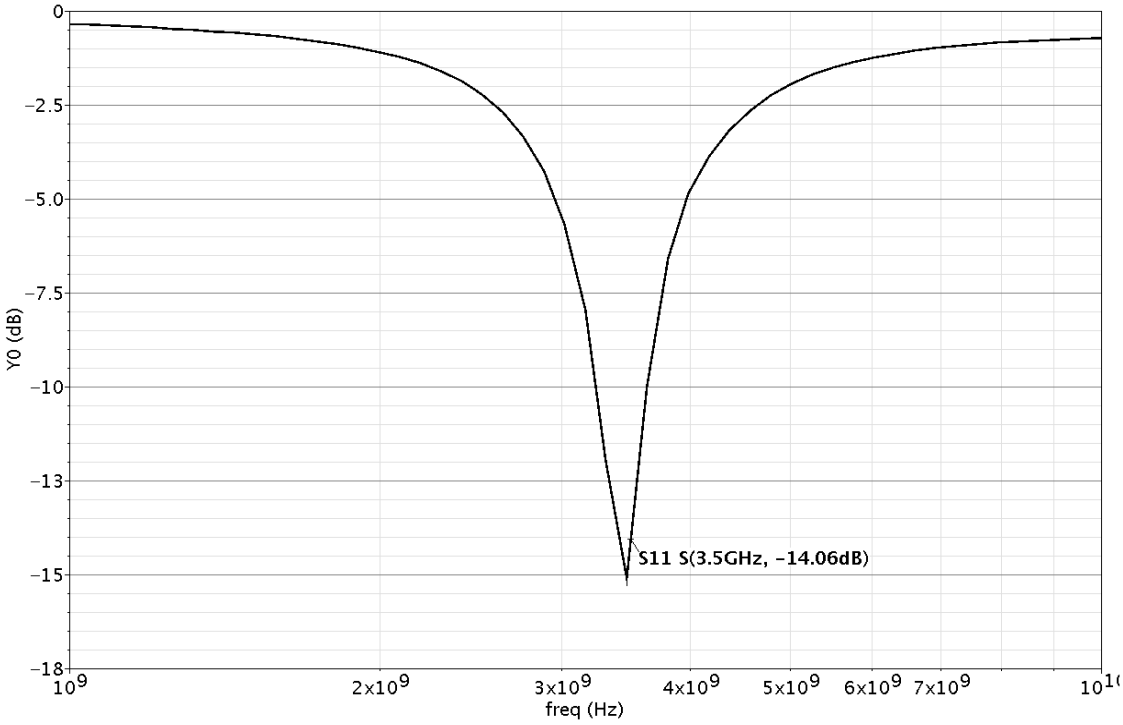


Fig. 5.4: simulation of Input return loss S11(schematic)

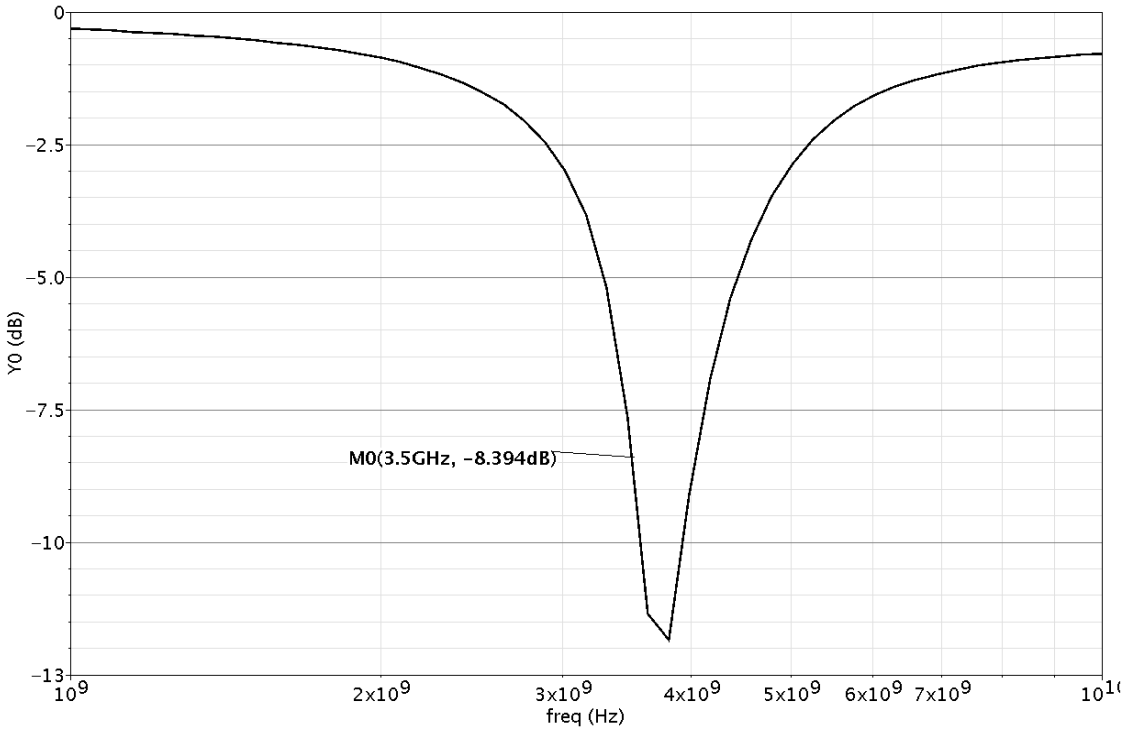


Fig. 5.5: simulation of Input return loss S11 (post layout)

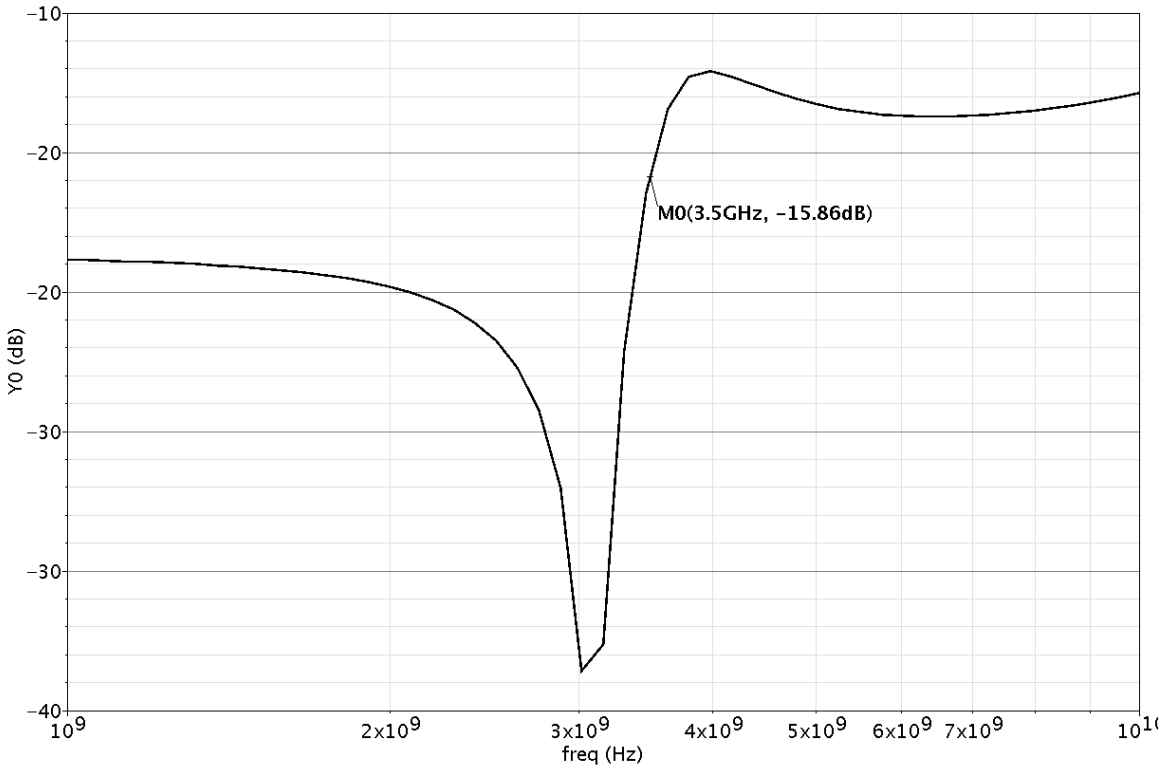


Fig. 5.6: Simulation of Output return loss S22 (Schematic)

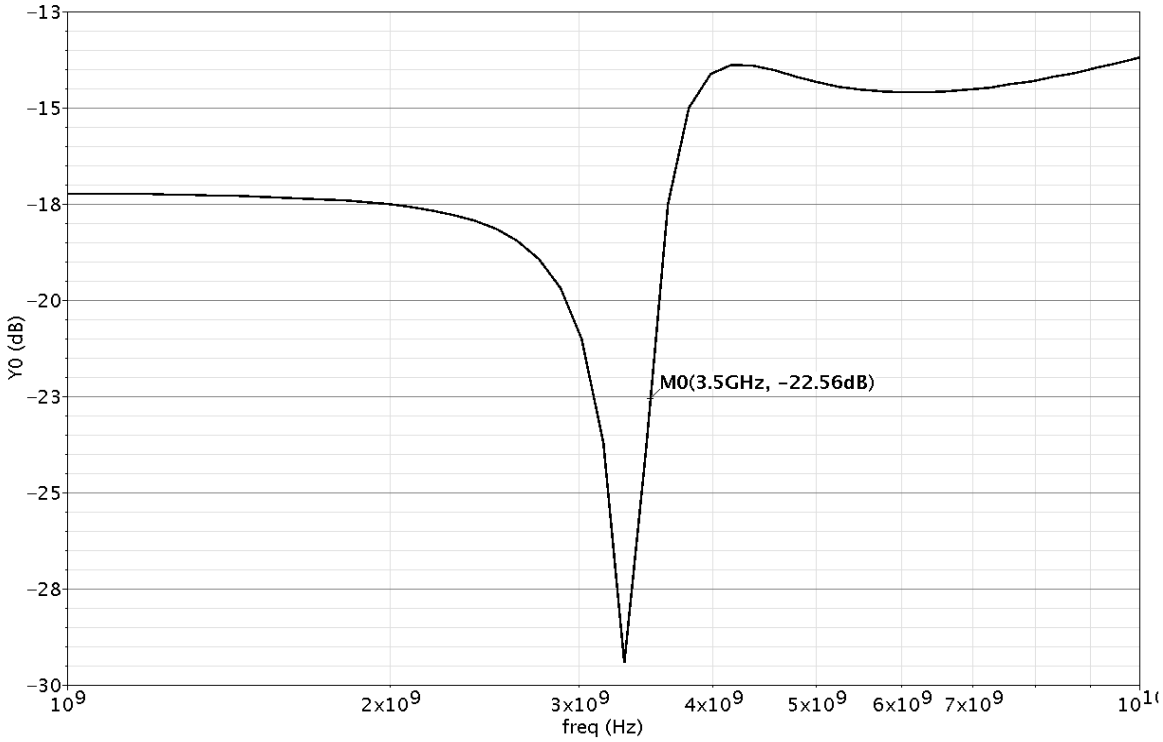


Fig. 5.7: Simulation of Output return loss S22 (post layout)

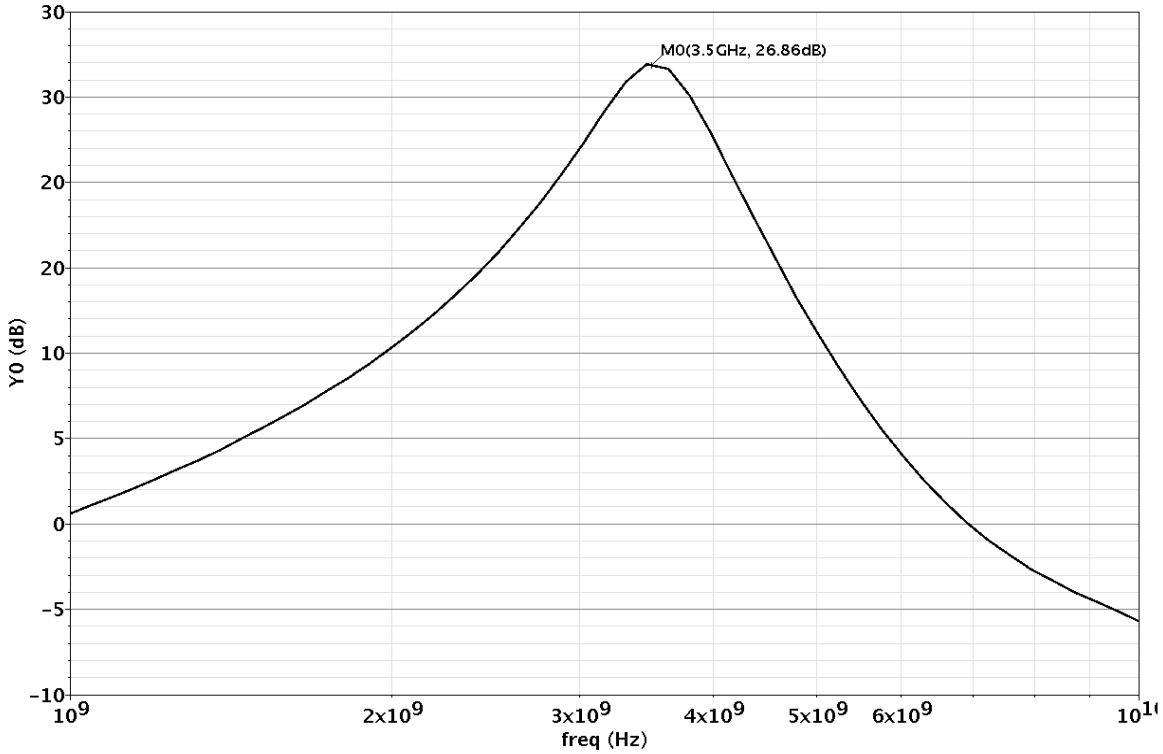


Fig. 5.8: Simulation of Forward gain S21 (Schematic)

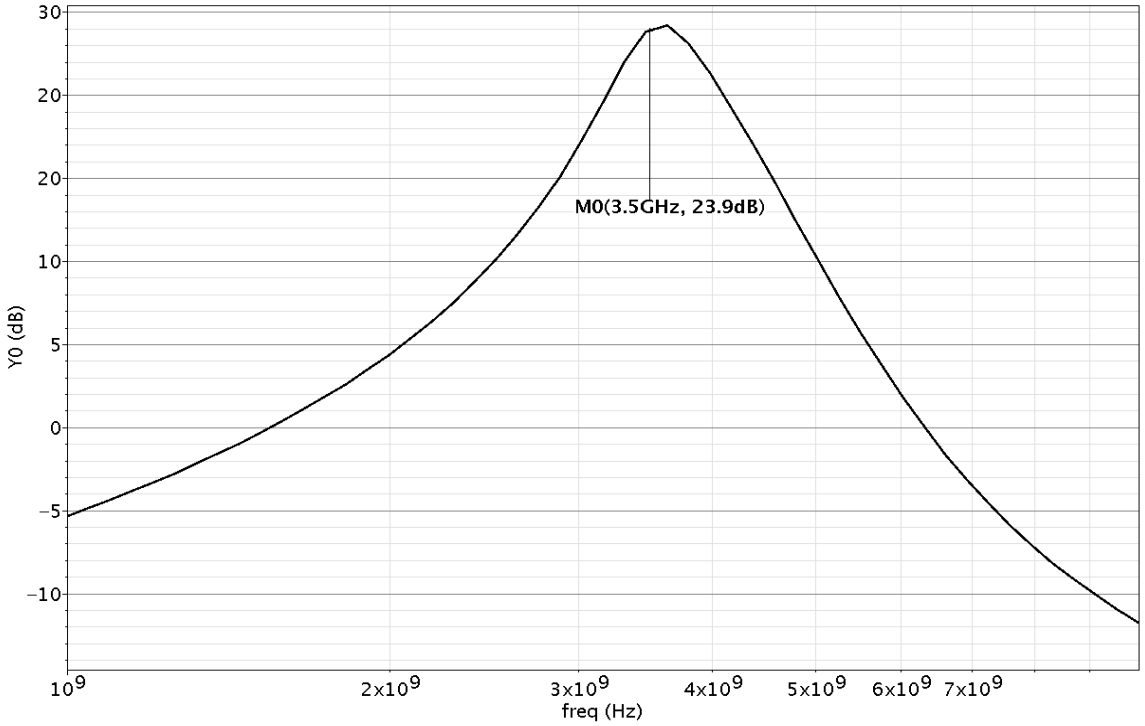


Fig. 5.9: Simulation of Forward gain S21 (Post layout)

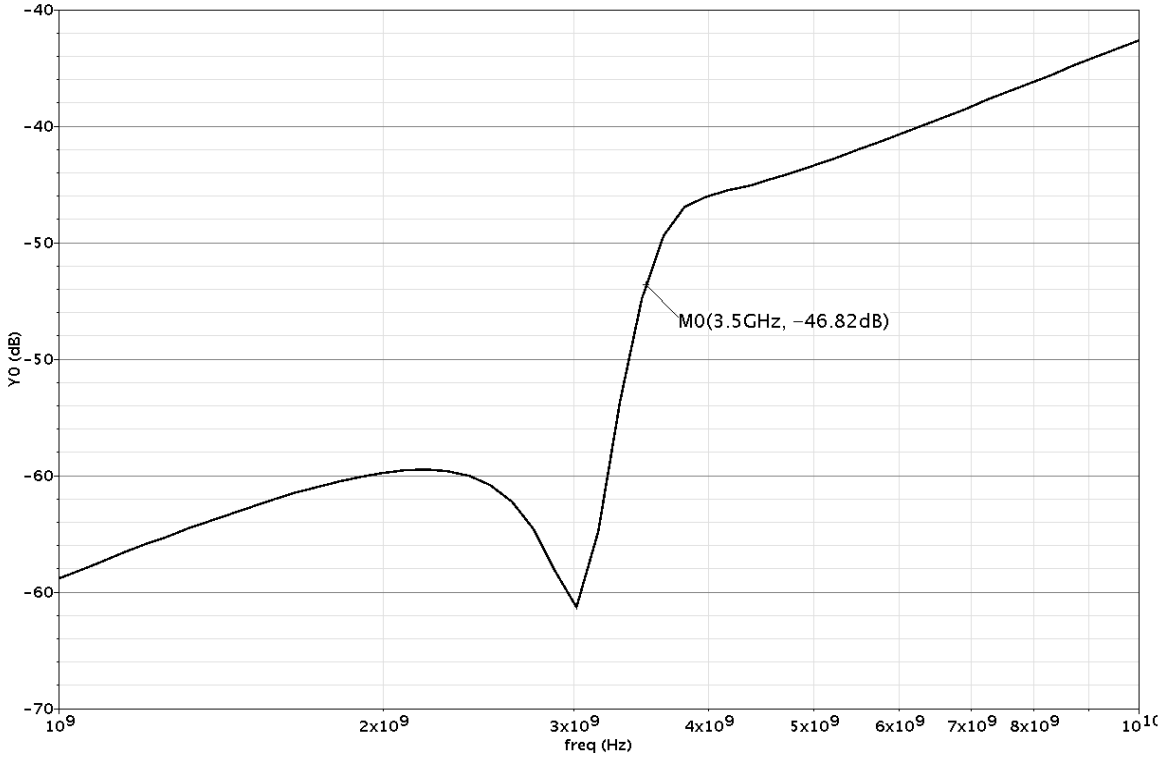


Fig. 5.10: Simulation of Reverse Isolation S12 (Schematic)

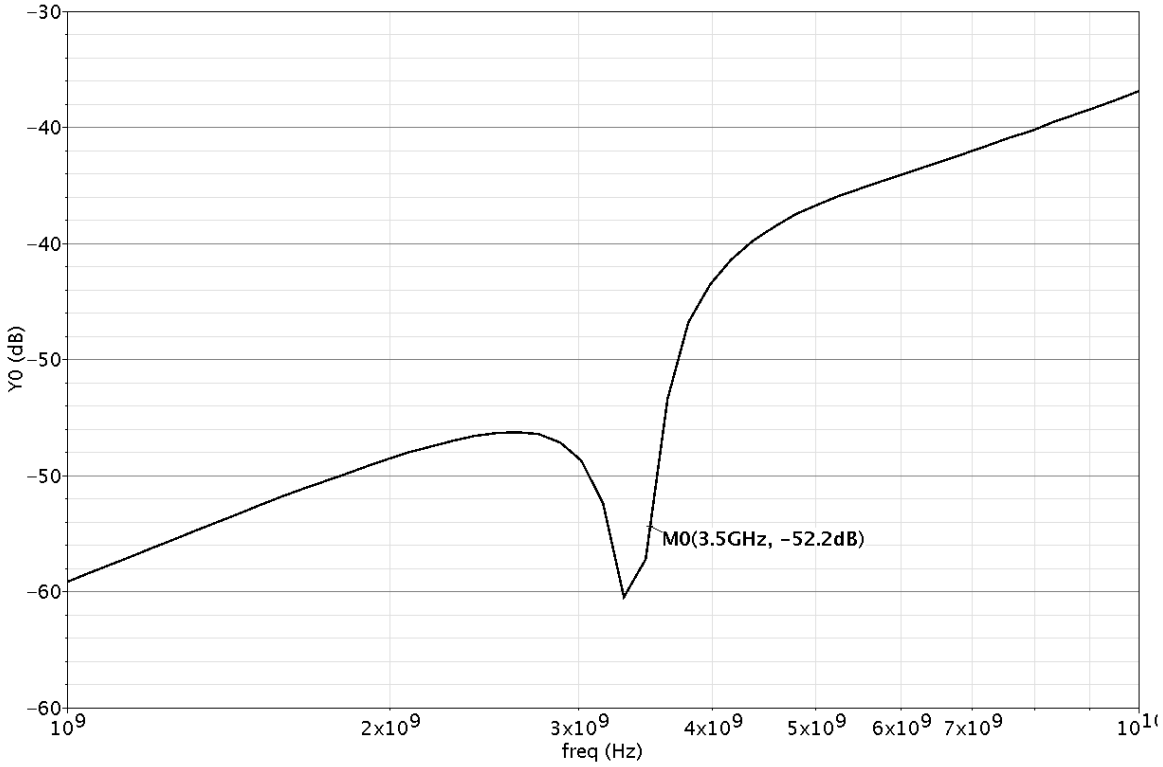


Fig. 5.11: Simulation of Reverse Isolation S12 (Post layout)

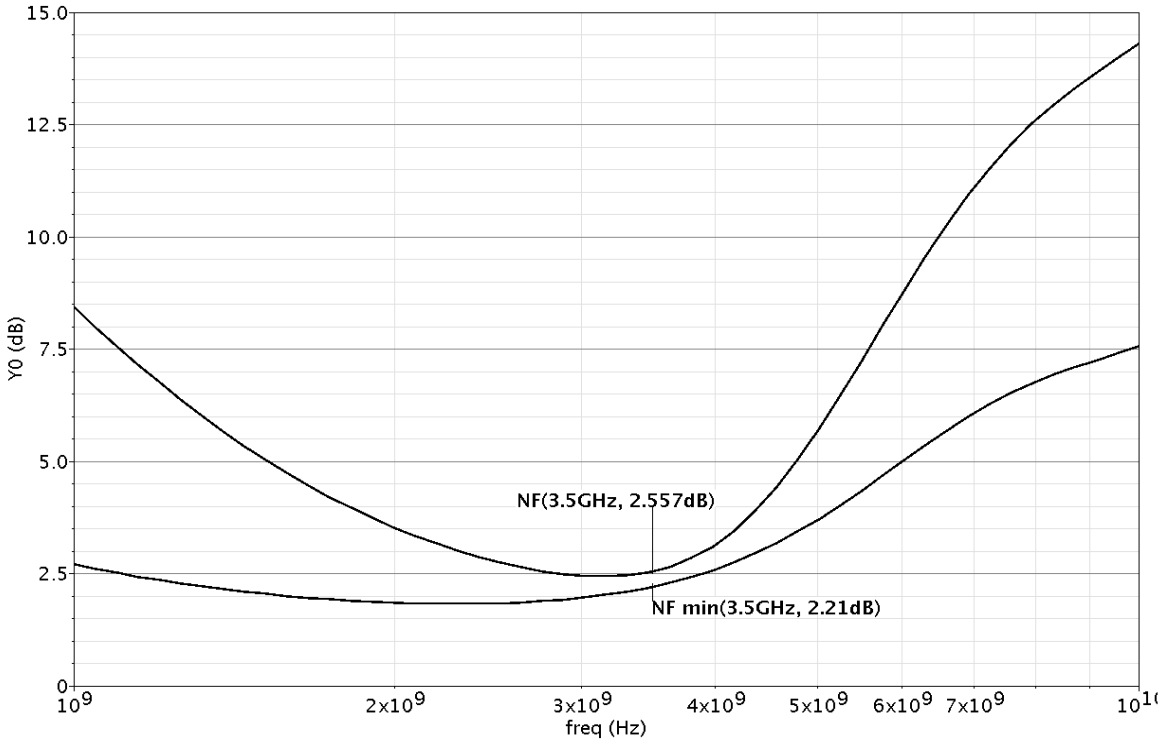


Fig. 5.12: Simulation of Noise Figure (Schematic)

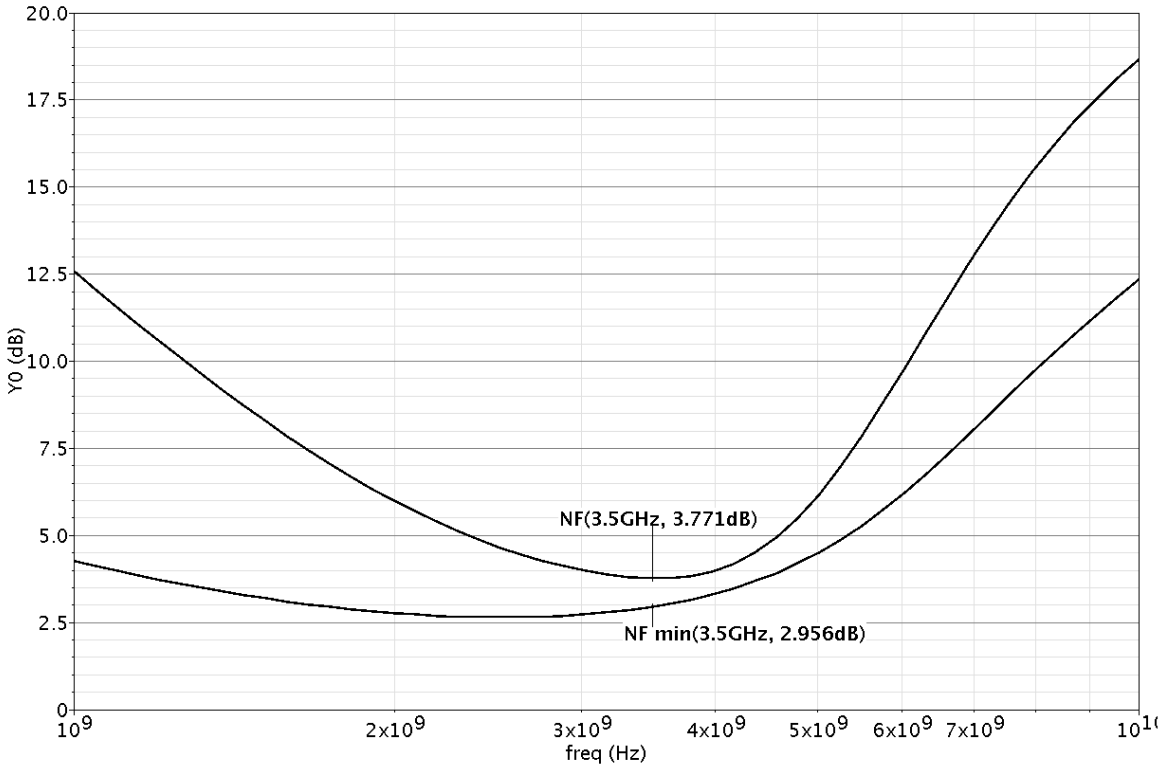


Fig. 5.13: Simulation of Noise Figure (Post layout)

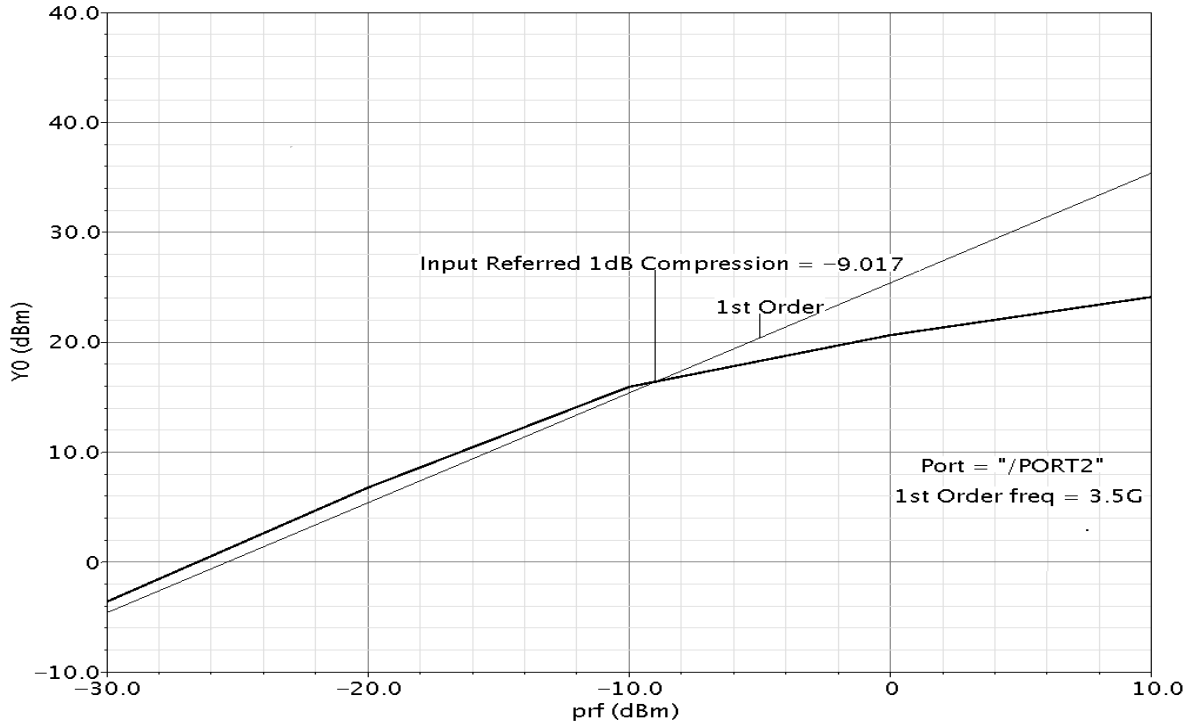


Fig. 5.14: Simulation of 1 – dB compression point (Schematic)

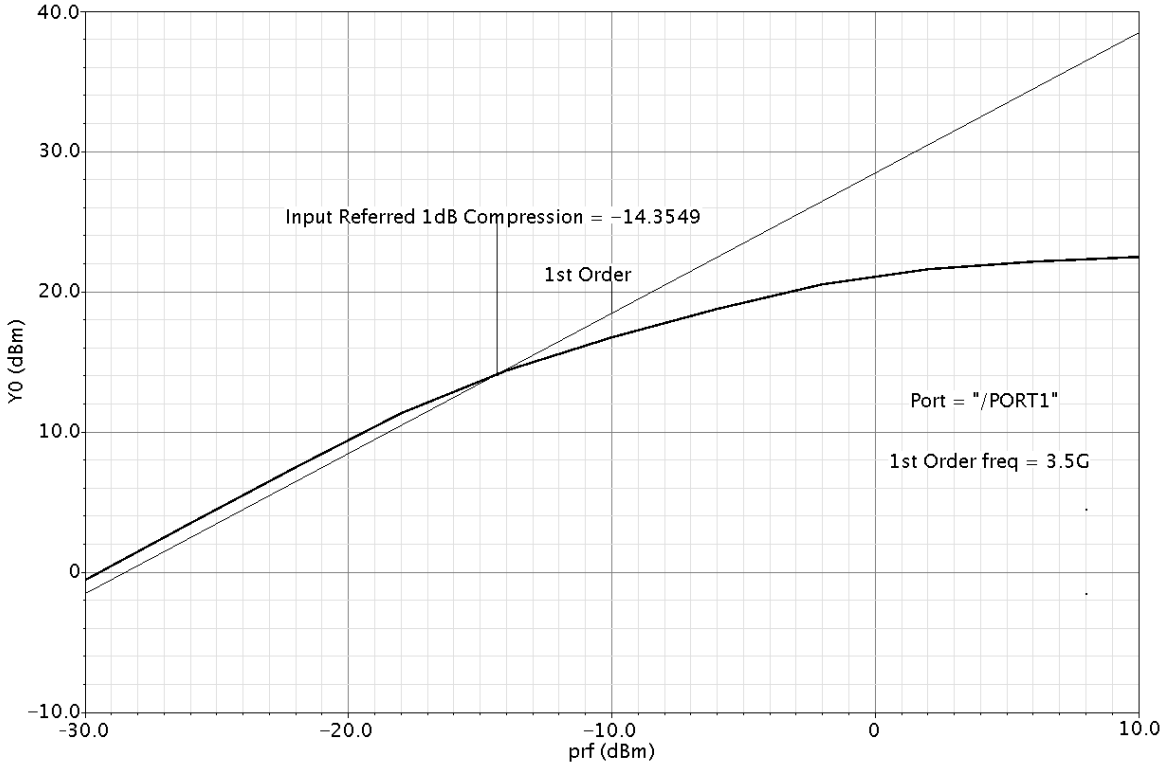


Fig. 5.15: Simulation of 1 – dB compression point (Post layout)

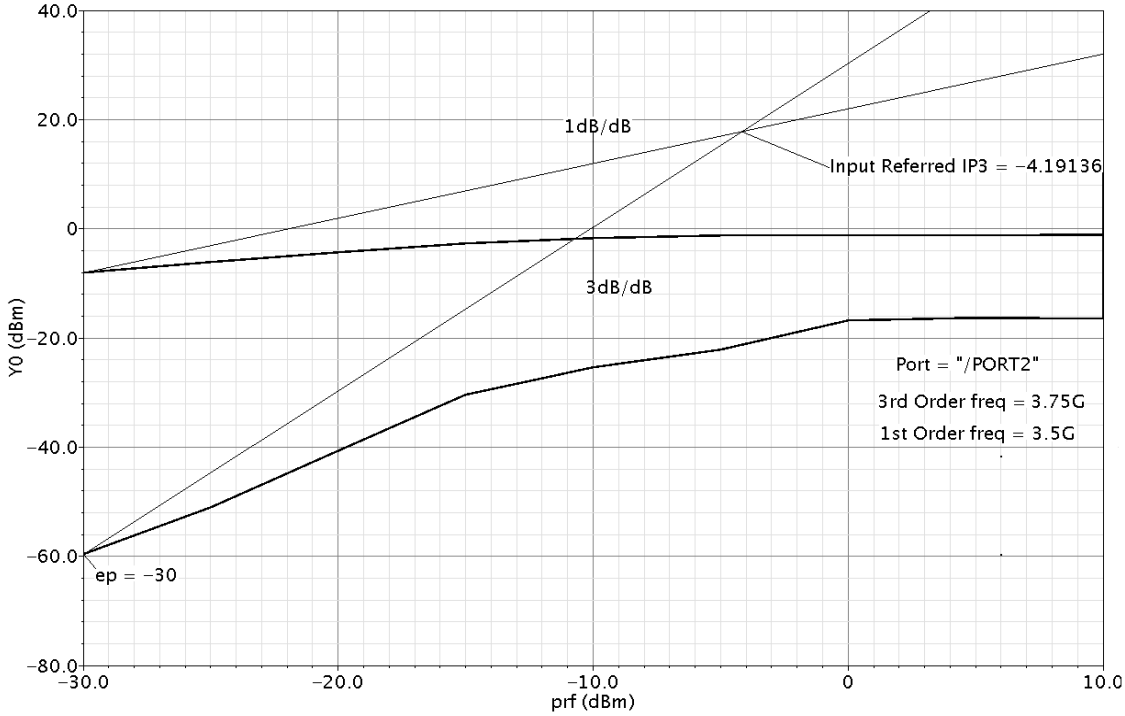


Fig. 5.16: Simulation of IIP3 (Schematic)

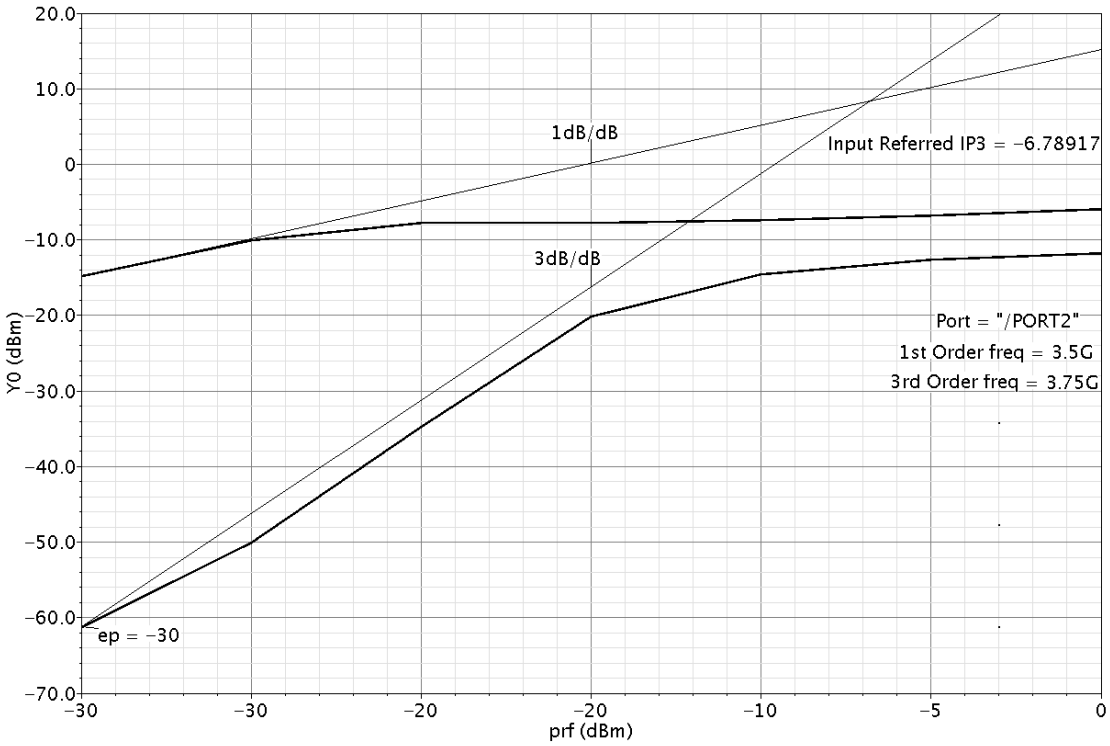


Fig. 5.17: Simulation of IIP3(Post layout)

Table 5.1: Summary of simulation Results for Enhanced cascode LNA

PARAMETER	Simple Cascode LNA	Enhanced Cascode LNA	
		Schematic	Post layout
S11(dB)	-25.53	-14.06	-8.39
S12(dB)	-39.61	-46.82	-52.2
S21(dB)	20.15	26.88	23.9
S22(dB)	-9.033	-15.86	-22.56
NF(dB)	2.749	2.557	3.771
NF min (dB)	2.194	2.21	2.956
1dB compression(dBm)	-17.8695	-9.017	-14.354
IIP3(dBm)	-11.9093	-4.1913	-6.7891

This design presents a 3.5 GHz LNA design using UMC 0.18µm CMOS technology. This enhanced cascade LNA requires a supply voltage of 1.8V and draws a current of 10.5mA, consumes 18.9 mw power, at 3.5GHz, this LNA has NF of 2.557dB, with input return loss of -14.06dB, output return loss of -15.86dB, and Forward gain of 26.88dB. This LNA performance shows high gain, with low NF. 1dB compression point of this design is -9.017dBm, means no gain compression for the received signals below compression point level. A two tone test is done to this LNA to observe the intermodulation, observed IIP3 is -4.1913dBm. This LNA can be used for high gain and low noise wireless applications. The performance summary is listed in Table 5.1.

6. Design of Differential LNA AT 3.5GHZ

6.1 Principle of operation of Differential LNA

Here, a 3.5 GHz LNA is designed based on source degenerative input matching cascade architecture with the 0.18um CMOS process. The architecture of designed differential LNA is shown in Fig. 6.1.The characteristic of this circuit is described below:

1. Two input double ended architecture is used in this design.
2. Design follows CMOS Cascode topology with source degeneration (Ls).
3. Biasing is provided by an active current mirror circuit at both the input terminals.
4. Proper output matching is provided using an extra buffer circuit at the output.

Cascade architecture reduces the Miller effect and provides improved S12. The source degeneration with the inductor provides good input matching as well as lower noise. The same was used in single ended cascade LNA. M4 and M5 are current mirrors and impedance R_{bais2} must be chosen large enough to reduce the further noise from the biasing stages. The active bias circuit are consist of transistor M5 and M6, impedance R_{bais1} and R_{bais2}, provides transistor M1 and M2 with gate current. M1 and M2 optimize the noise and the gain, and we must choose proper width for the transistor M1.

In order to cut the extra power added by biasing circuits, the width of transistors M5 and M6 has to be chosen a fraction of the M1 and M2 width, and bias impedance R_{bais2} should be large enough. Cin1, Cin2, Cout1, Cout2 are blocking capacitors. The value of series resonance inductors Ls1, Ls2, Ls3, Ls4 added in this circuit are to be chosen based on the iterative simulations until it reaches the proper gain without degrading the input and output match. The added buffer outside the circuit is helpful in attaining the best output match and load tuning.

Next section shows the pre and post layout simulation results of the designed circuits. Fig 6.1 shows the architecture of the Designed Differential LNA design.

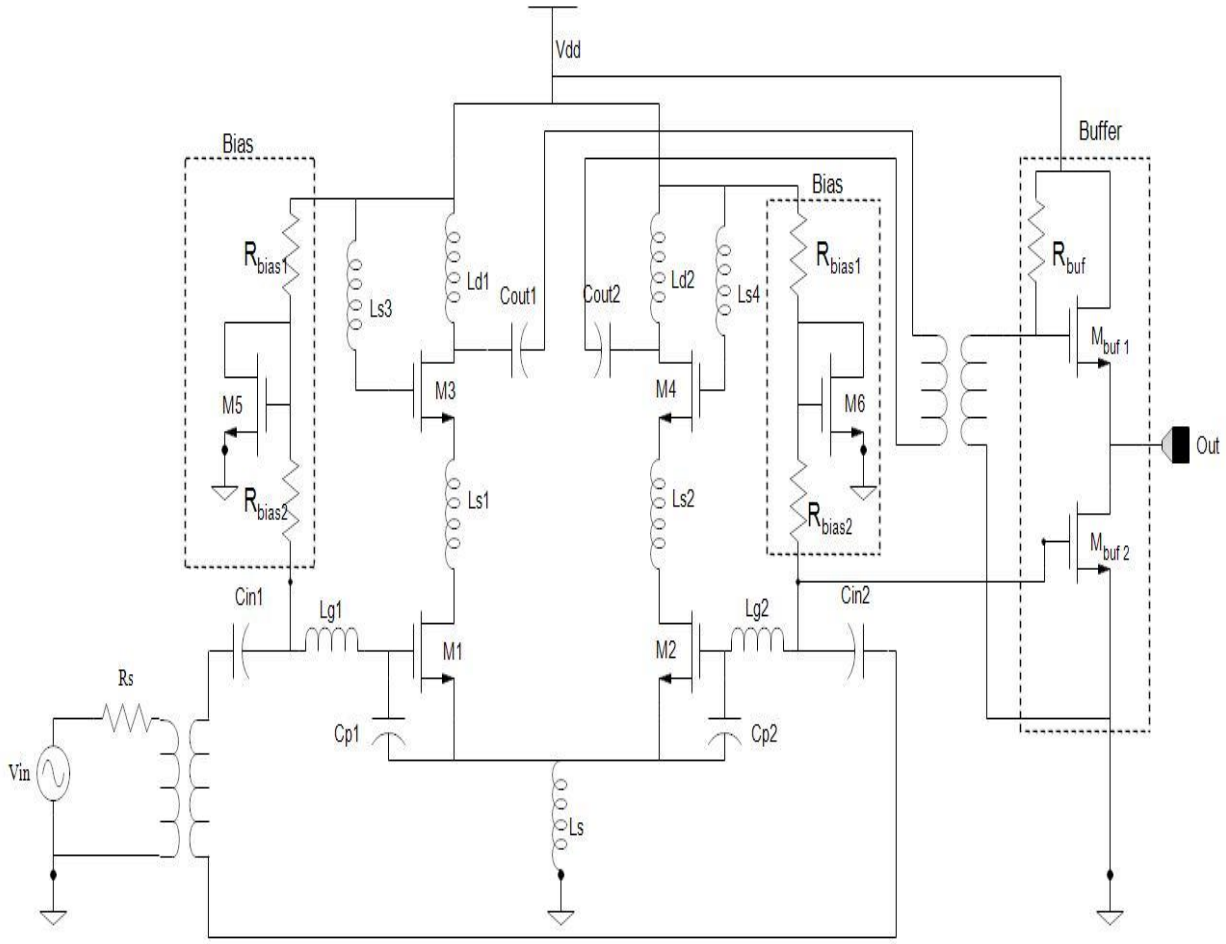


Fig. 6.1: Architecture of Differential CMOS LNA

6.2 Simulation Results

The designed LNA at 3.5GHz, shown in Fig. 6.1, was simulated using the cadence 0.18µmc RF spectre tool. Schematic and layout diagrams are shown in Fig 6.2 and 6.3 respectively. Pre and post layout Simulation results are shown in 6.4 -6.17. From the following simulation results, we can observe a small difference between pre and post layout curves, because of parasitics formed during the layout process.

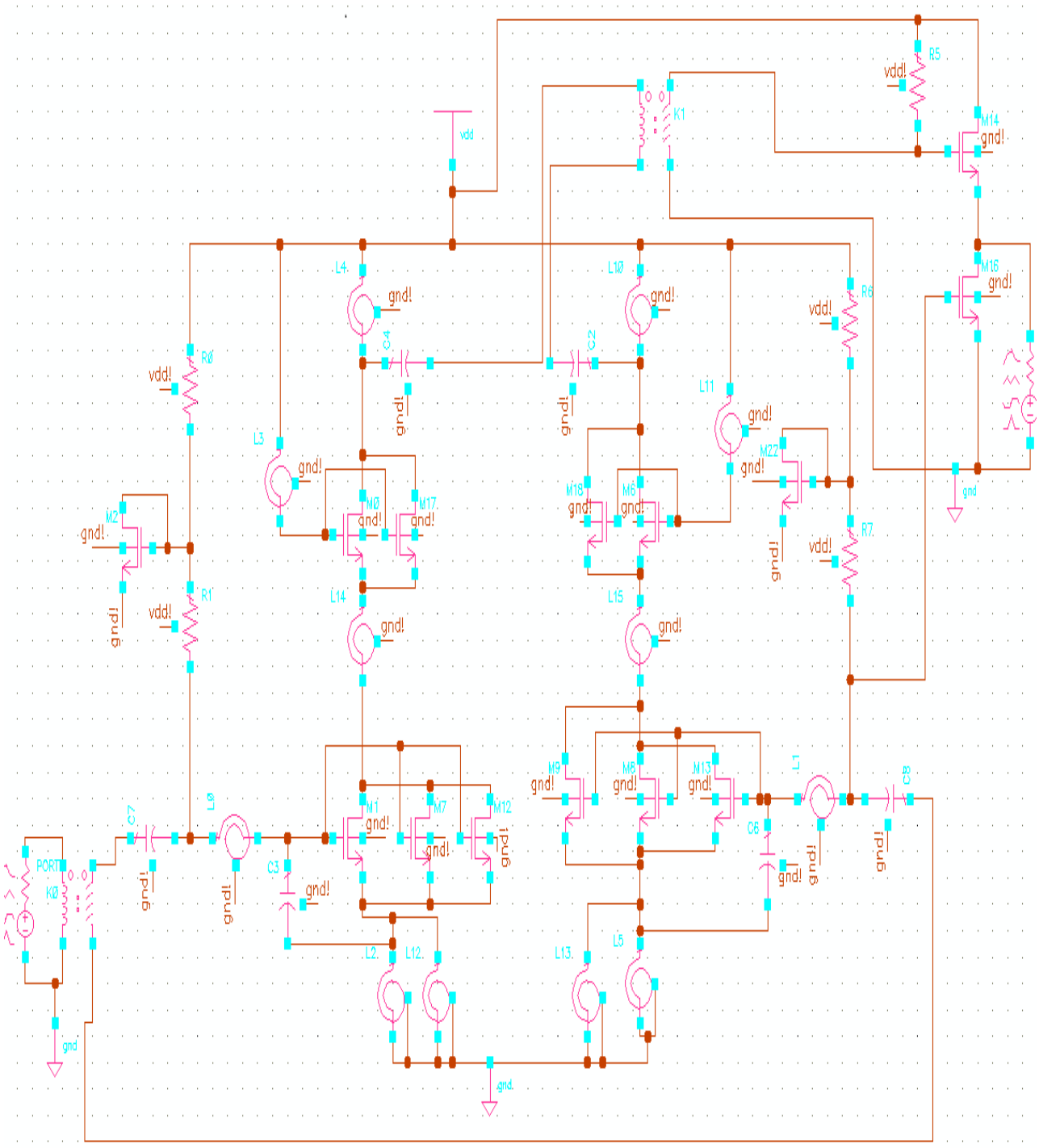
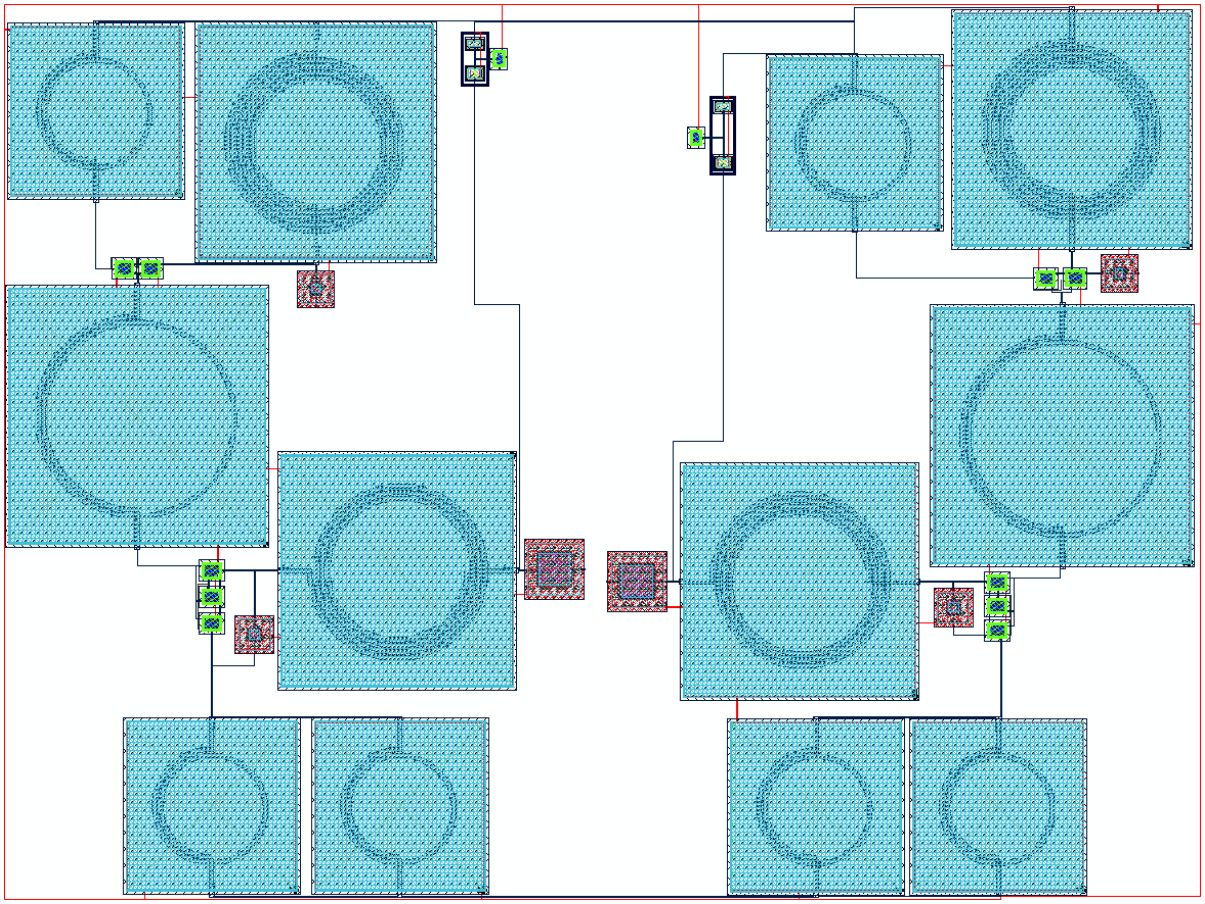
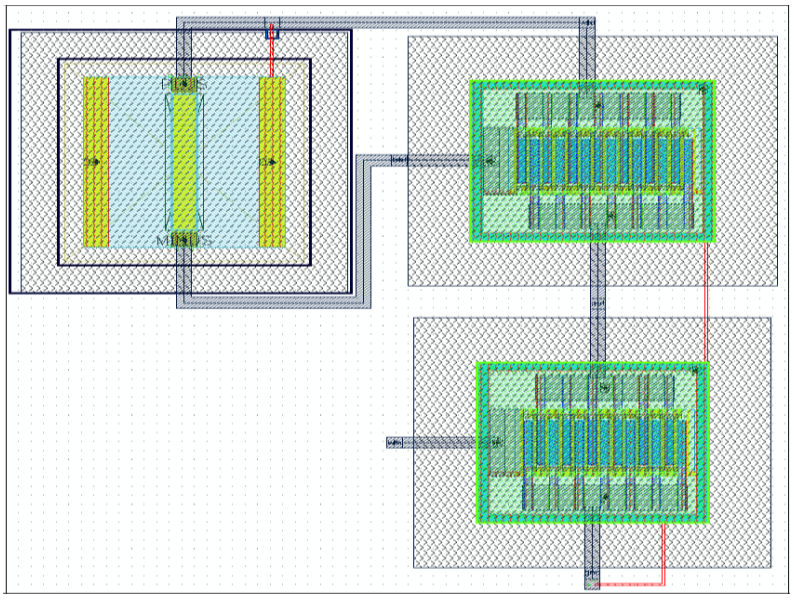


Fig 6.2: Schematic of Designed Differential cascode LNA at 3.5GHz



(a)



(b)

Fig. 6.3: Layout of the Differential LNA (a) Double ended diff. LNA (b) Buffer

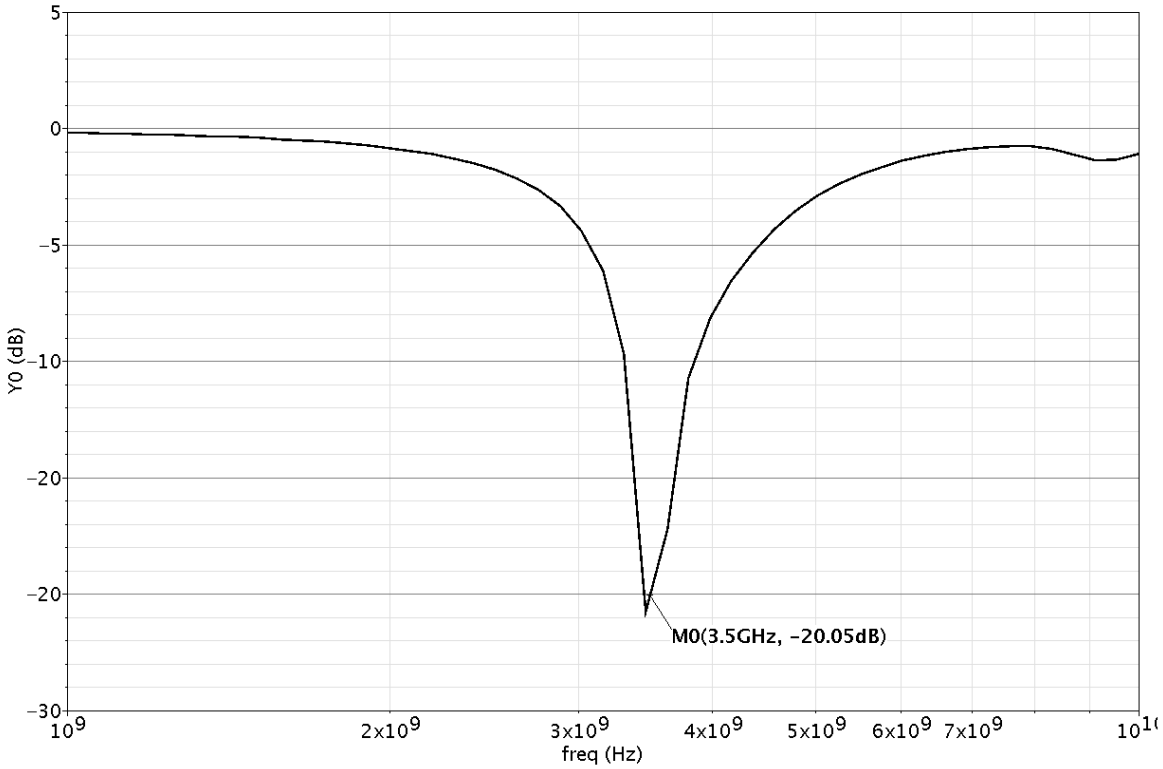


Fig. 6.4: simulation of Input return loss S11(schematic)

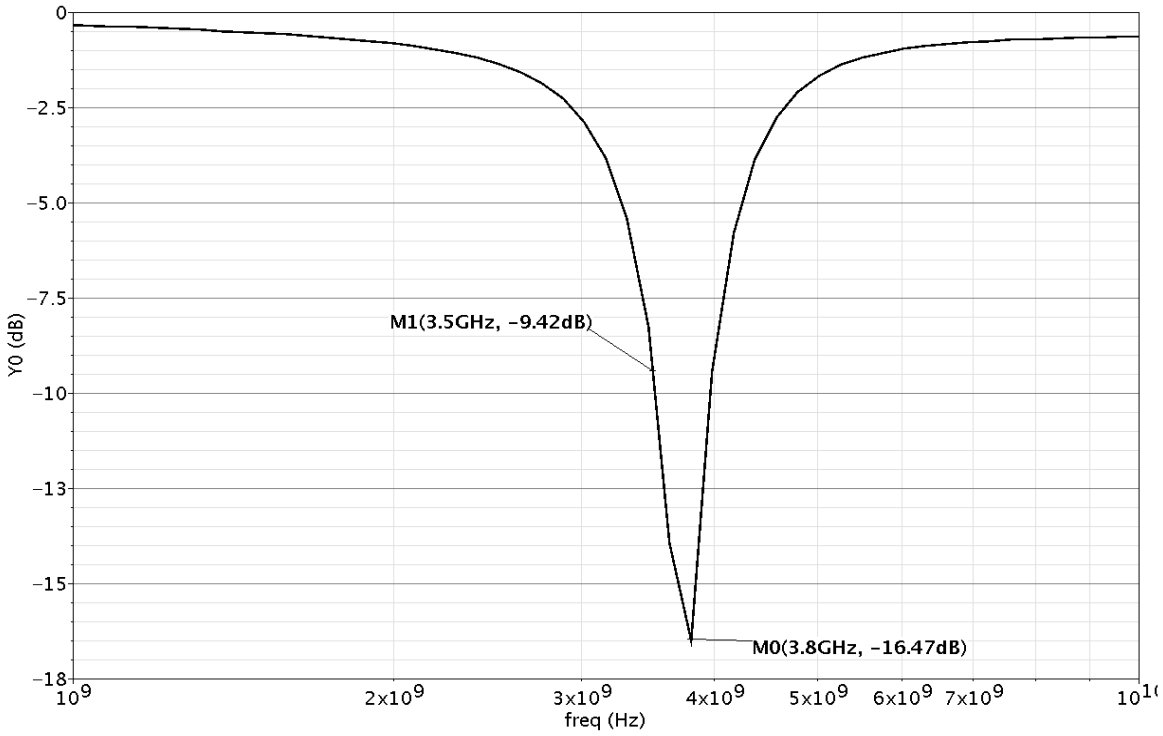


Fig. 6.5: simulation of Input return loss S11 (post layout)

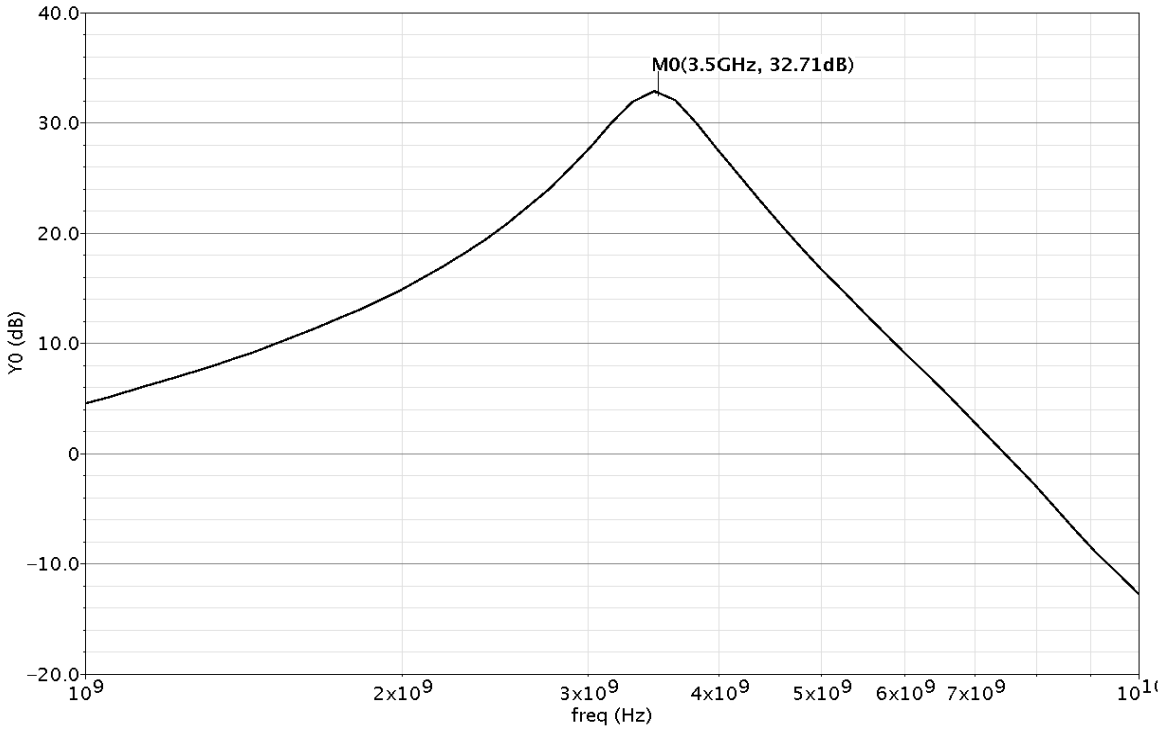


Fig. 6.6: Simulation of Forward gain S21 (Schematic)

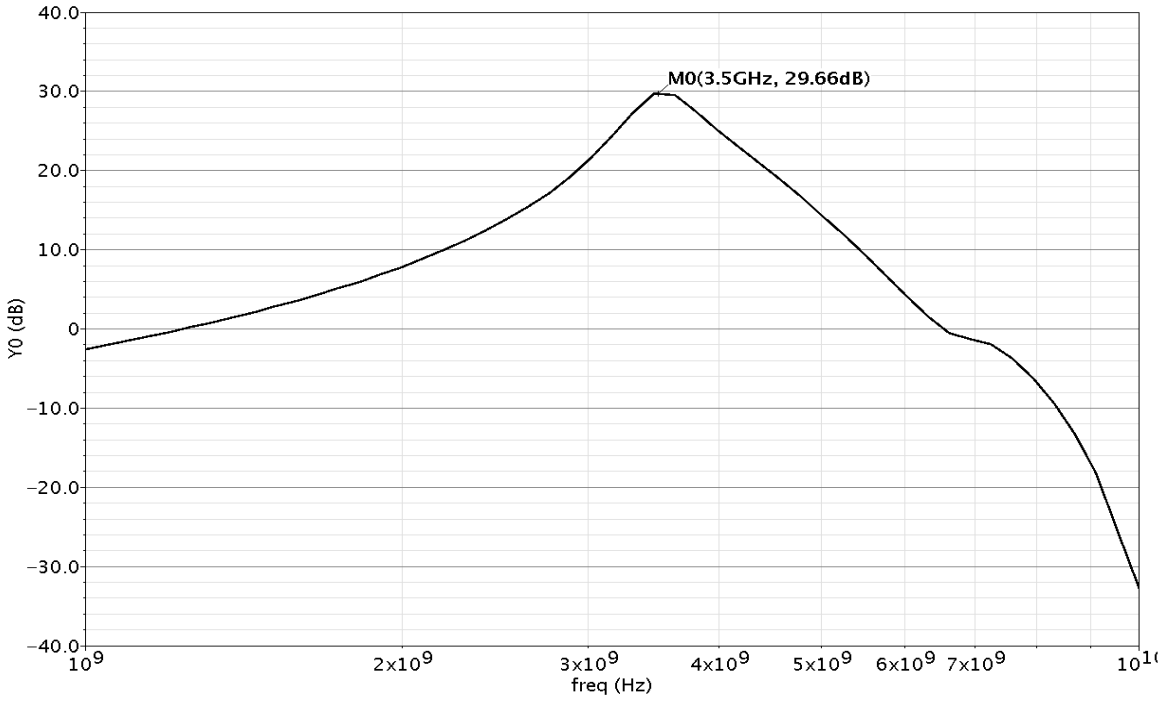


Fig. 6.7: Simulation of Forward gain S21 (Post layout)

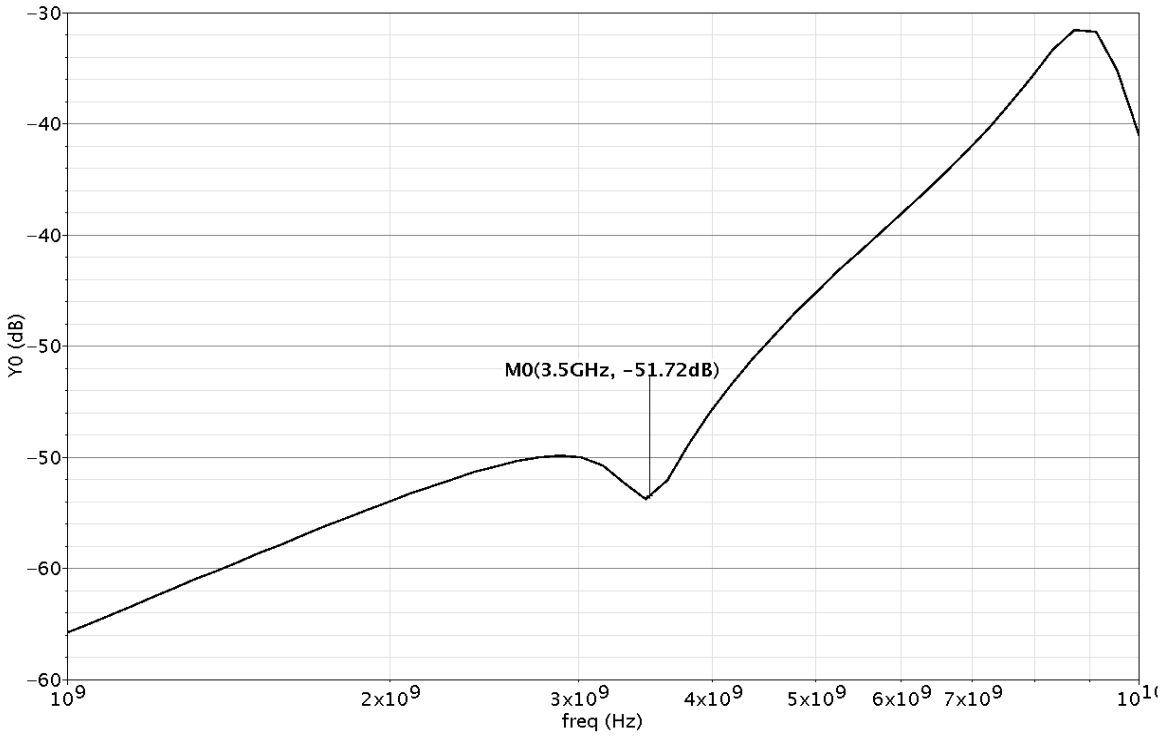


Fig. 6.8: Simulation of Reverse Isolation S12 (Schematic)

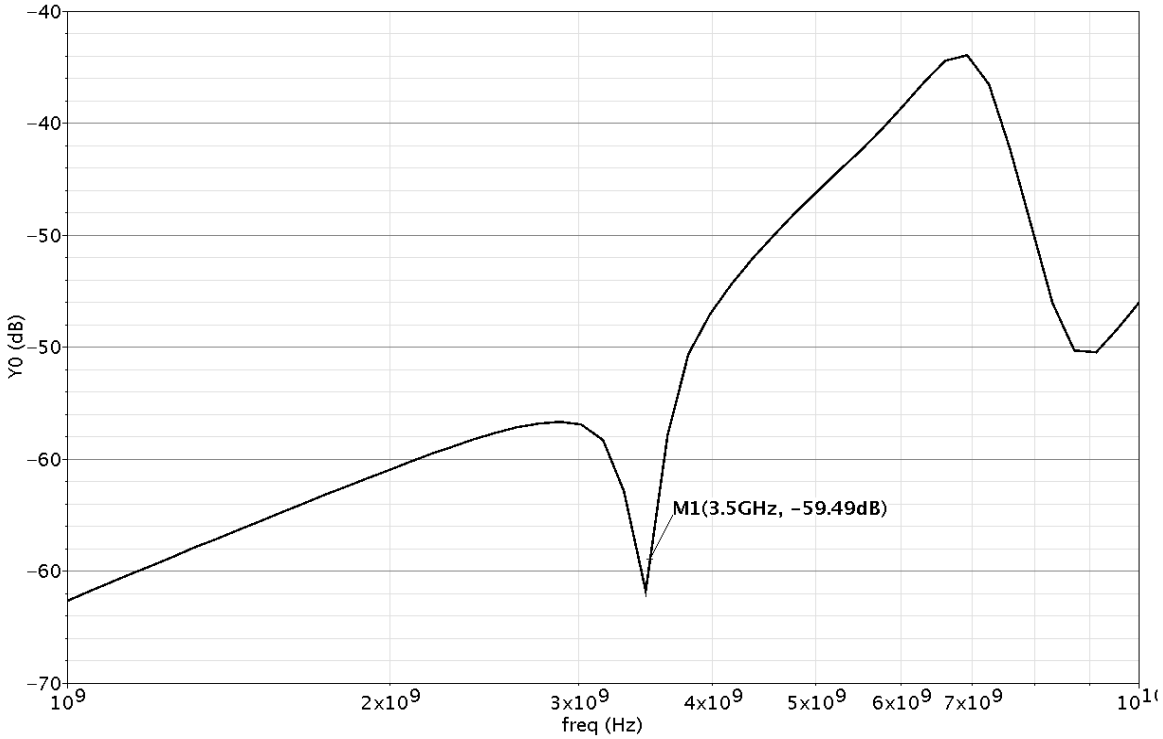


Fig. 6.9: Simulation of Reverse Isolation S12 (Post layout)

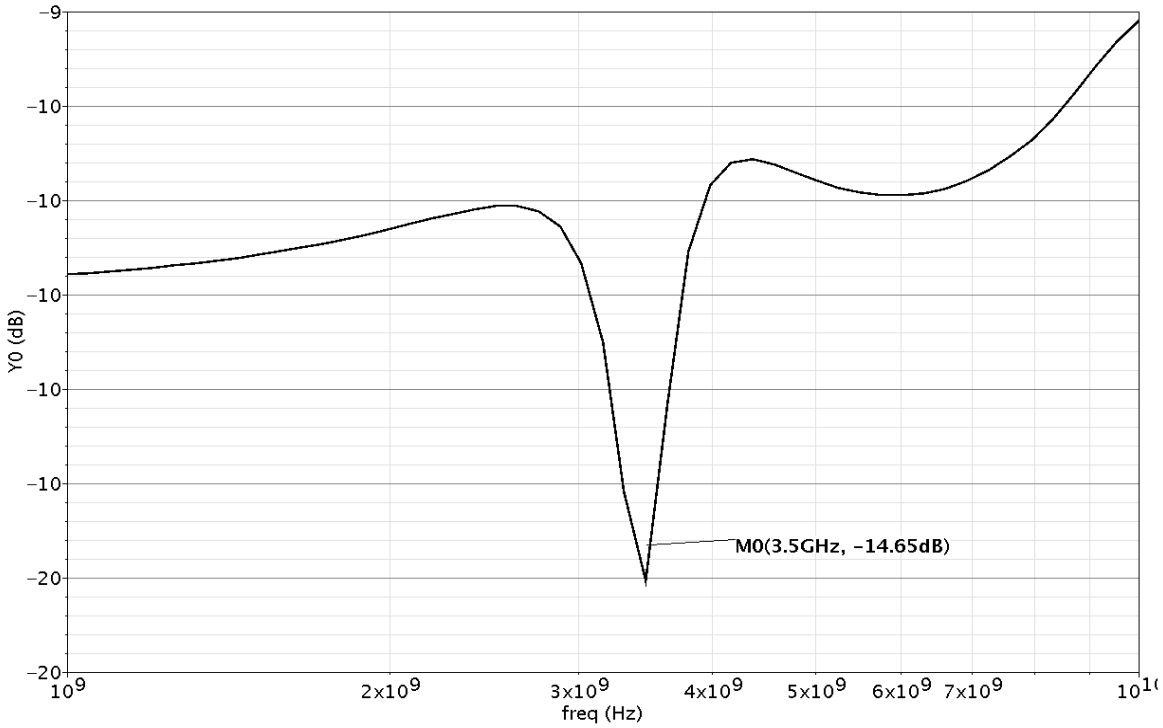


Fig. 6.10: Simulation of Output return loss S22 (Schematic)

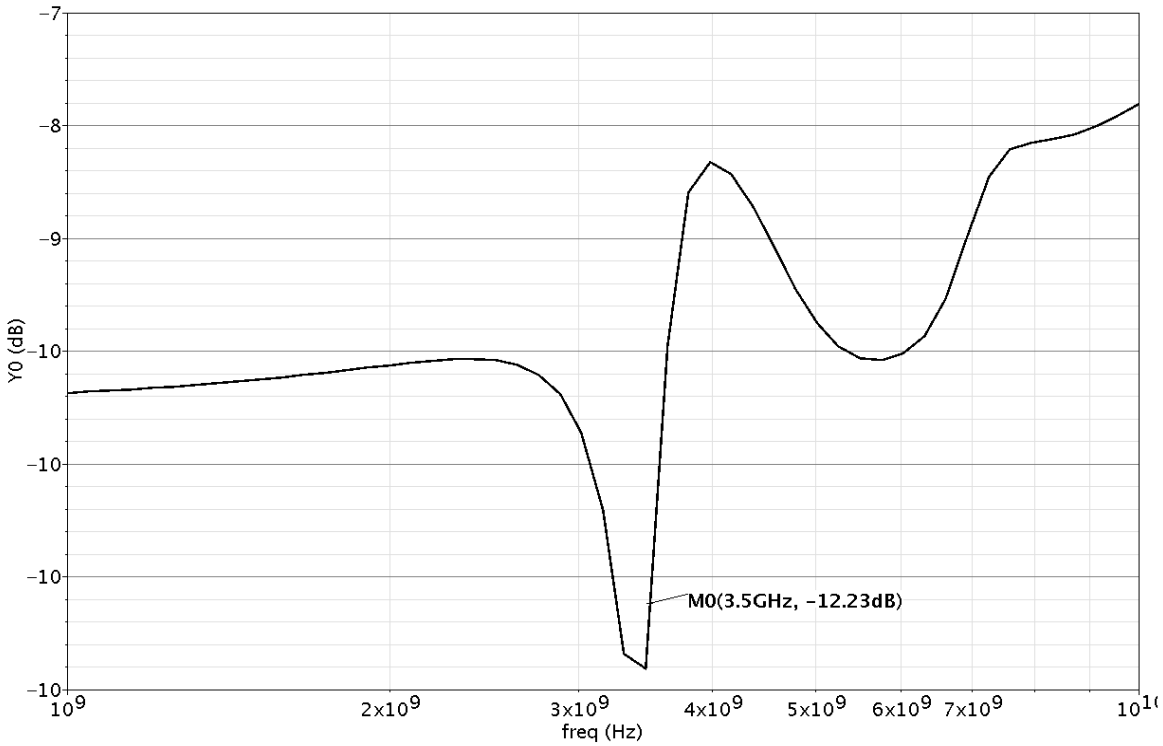


Fig. 6.11: Simulation of Output return loss S22 (Post layout)

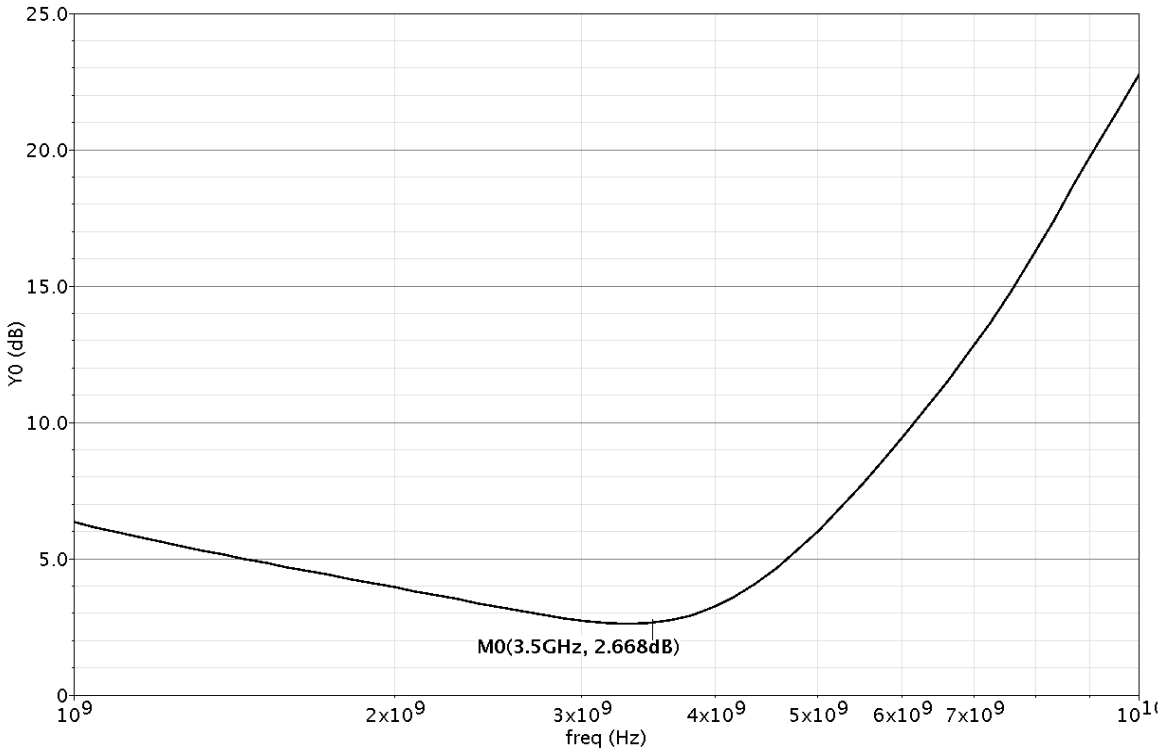


Fig. 6.12: Simulation of Noise Figure (Schematic)

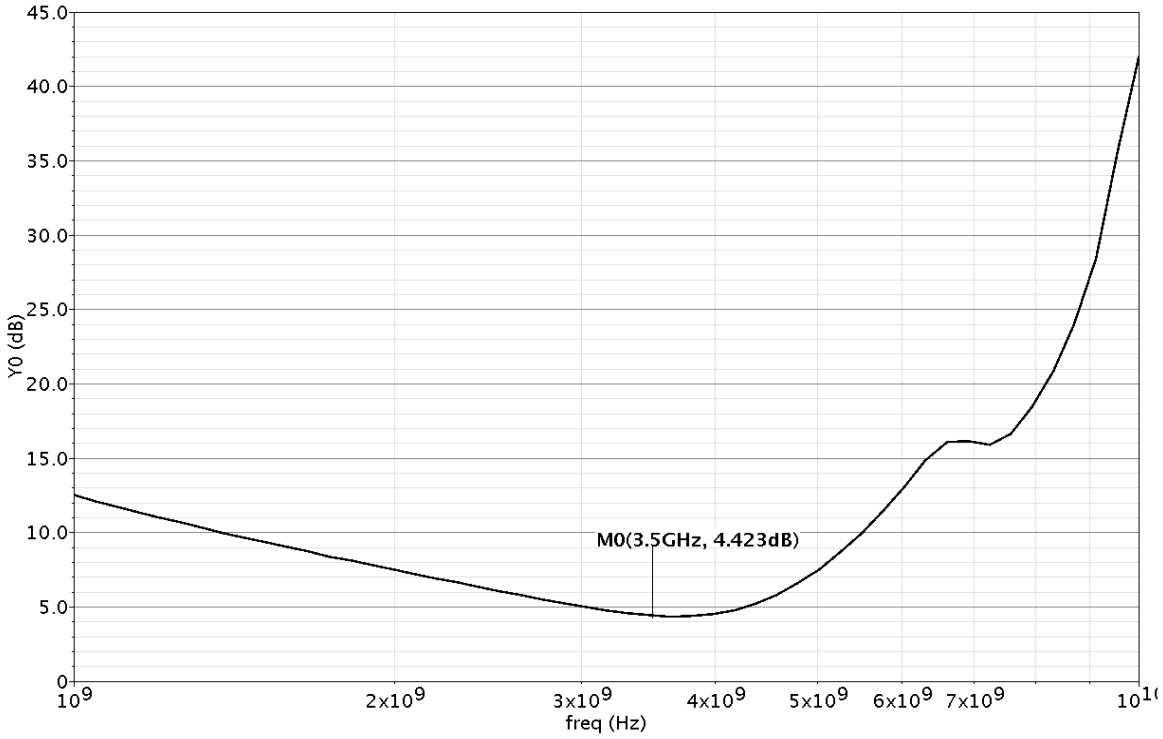


Fig. 6.13: Simulation of Noise Figure (Post layout)

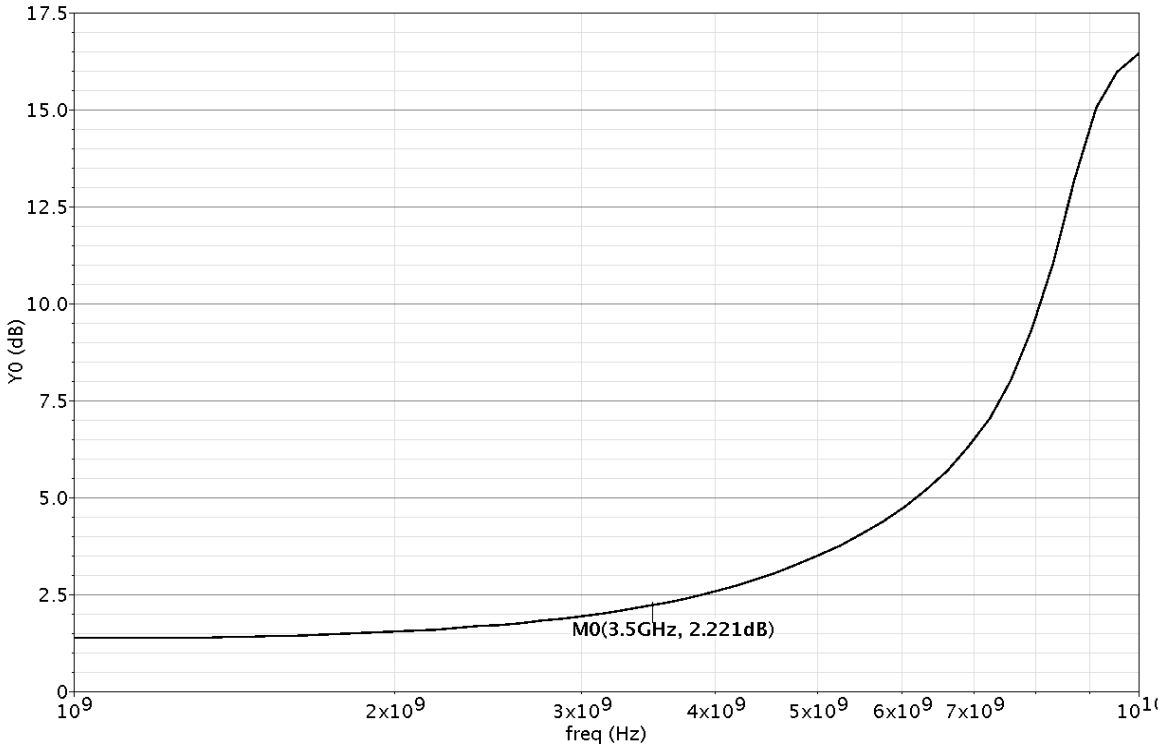


Fig. 6.14: Simulation of minimum NF (Schematic)

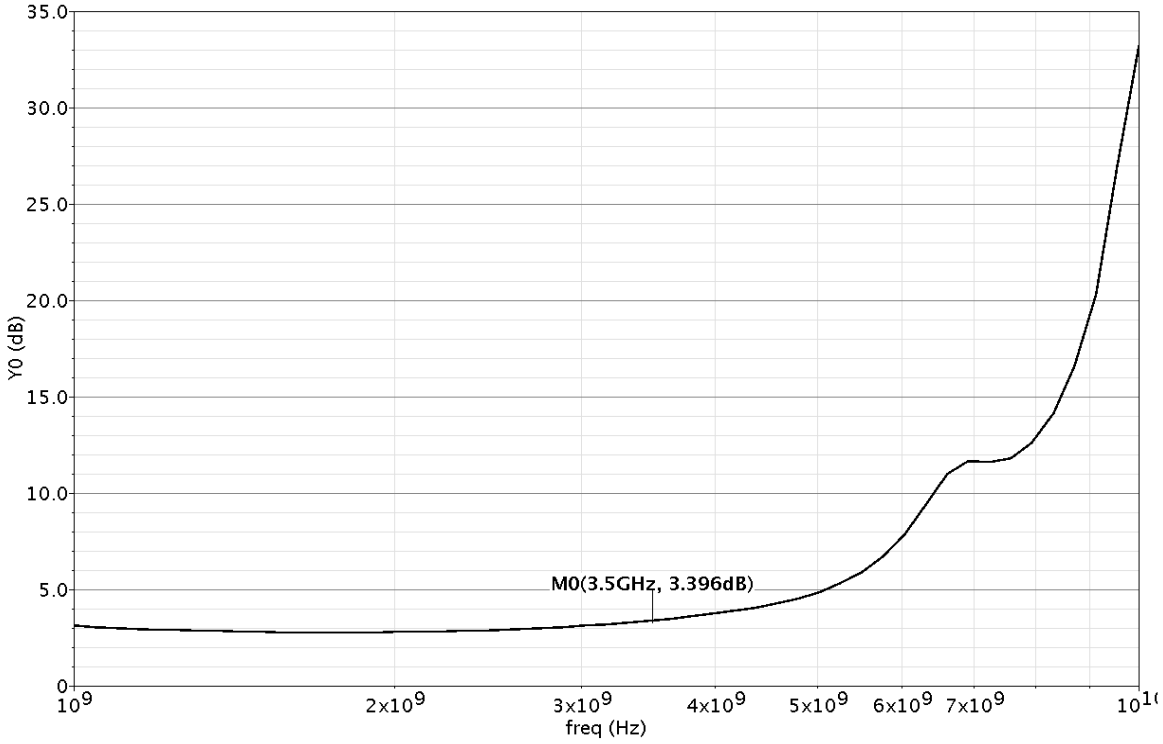


Fig. 6.15: Simulation of minimum NF (Post layout)

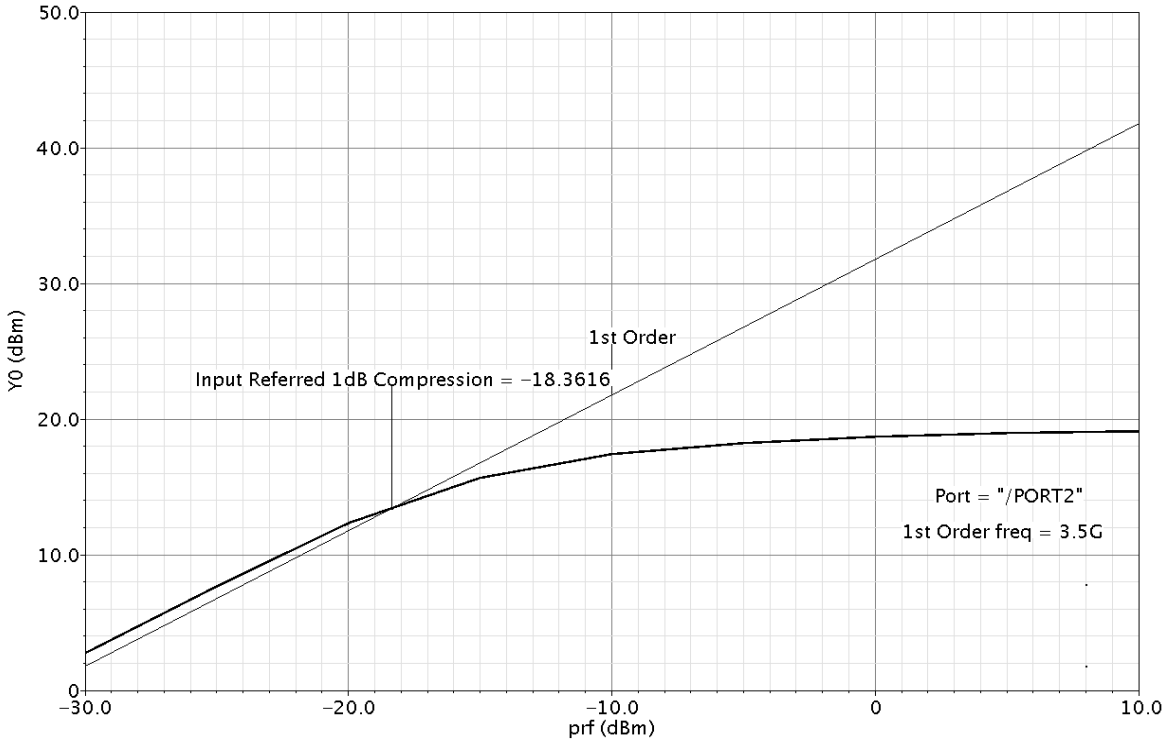


Fig. 6.16: Simulation of 1 – dB compression point (Schematic)

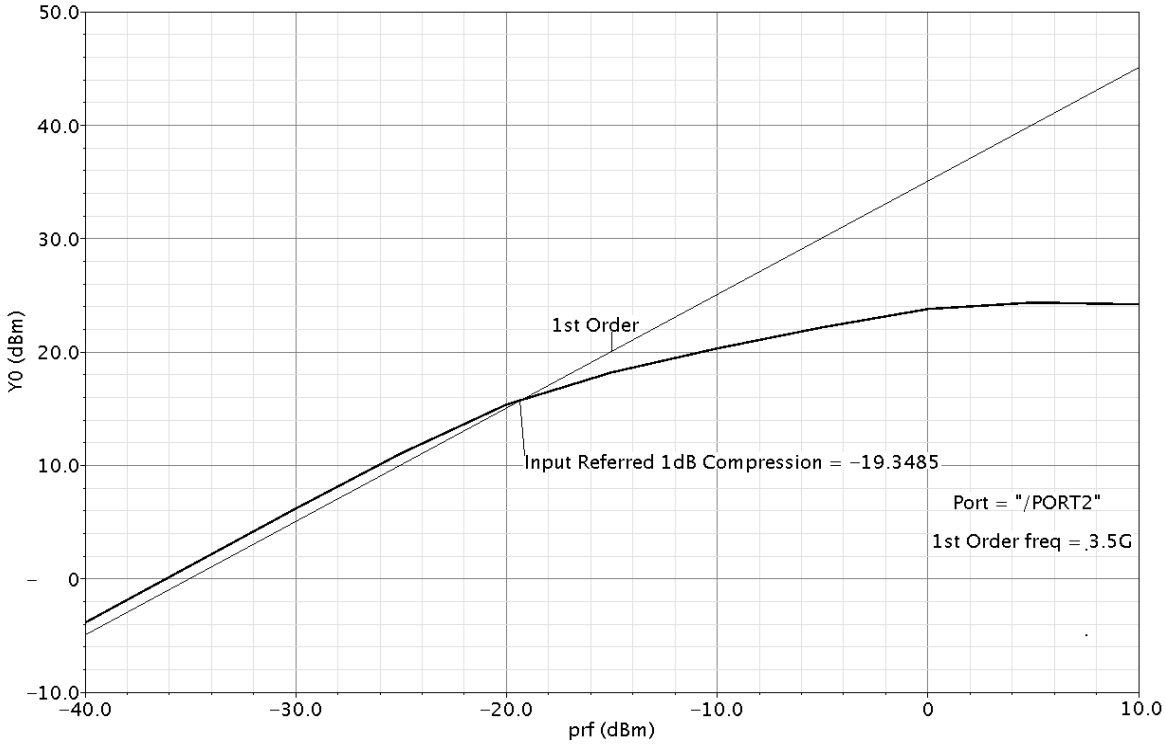


Fig. 6.17: Simulation of 1 – dB compression point (Post layout)

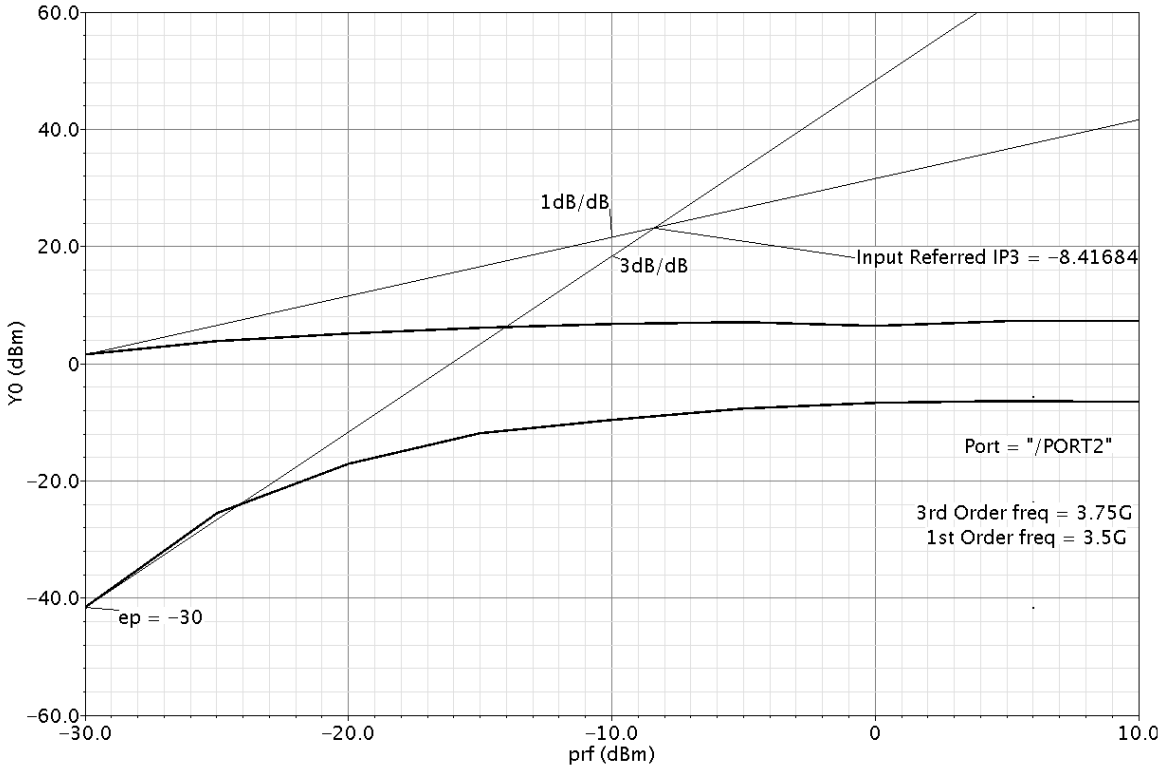


Fig. 6.18: Simulation of IIP3 (Schematic)

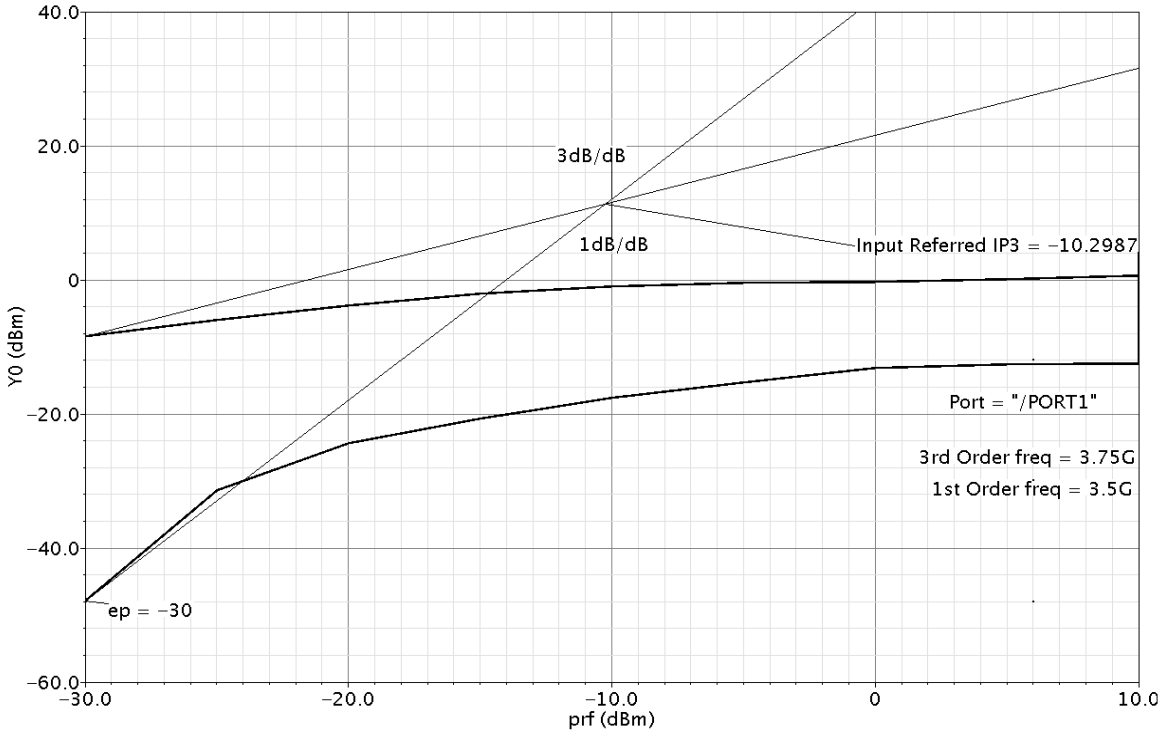


Fig. 6.19: Simulation of IIP3(Post layout)

Table 6.1: Summary of simulation Results for differential LNA at 3.5GHz

PARAMETER	Enhanced Cascode LNA		Differential LNA	
	Schematic	Post layout	Schematic	Post layout
S11(dB)	-14.06	-8.39	-20.05	-9.42
S12(dB)	-46.82	-52.2	-51.72	-59.49
S21(dB)	26.88	23.9	32.71	29.66
S22(dB)	-15.86	-22.56	-14.65	-12.23
NF(dB)	2.557	3.771	2.668	4.423
NF min (dB)	2.21	2.956	2.221	3.396
1dB compression(dBm)	-9.017	-14.354	-18.361	-19.348
IIP3(dBm)	-4.191	-6.789	-8.416	-10.298

This chapter presents a 3.5 GHz differential LNA design using UMC 0.18μm CMOS process. This differential LNA requires a supply voltage of 1.8V. This LNA has NF of 2.668dB, with input return loss of -20.05dB, output return loss of -14.65dB, and Forward gain of 32.71dB. This differential LNA performance represents high gain, with low noise figure. 1dB compression point of this design is -18.361dBm, means no gain compression for the received signals below compression point level. A two tone test is done to this LNA to observe the intermodulation, observed IIP3 is -8.416dBm. This LNA can be used in wireless applications for high gain. The performance summary is listed in Table 6.1.

CONCLUSION

In this Thesis, the design of high gain source degenerated CMOS cascade LNA and its enhanced version are discussed. A Differential LNA model with the same concept at 3.5GHz for Wi-MAX applications is presented. This designs were implemented in Cadence 0.18µmc RF CMOS technology. All the designs operate with the 1.8 V supply voltage. These LNAs give high gain, low noise figure with proper input and output matching, also the inter modulation is reduced to an extent. These LNAs can be used in applications where high gain and low noise figure are needed.

FUTURE WORK

- The difference between the pre and Post layout results can be further reduced.
- The Intermodulation (IIP3) as well as linearity can be improved.
- Power consumption can be reduced further.
- Noise Figure of the designs can be reduced.

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